INTEGRATED CIRCUITS

DATA SHEET

MB2245

16-bit transceivers with direction pins (3-State)

Product specification Supersedes data of 1993 Aug 18 IC23 Data Handbook





16-bit transceiver with direction pins (3-State)

MB2245

FEATURES

- 16-bit bidirectional bus interface
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The MB2245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive

The MB2245 device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable (1OE, 2OE) inputs for easy cascading and two Direction (1DIR, 2DIR) inputs for direction control.

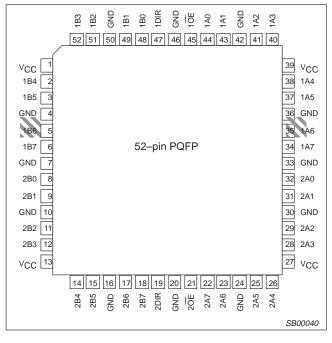
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C; GND = 0V	TYPICAL	UNIT
^t PLH ^t PHL	Propagation delay nAx to nBx or nBx to nAx	$C_L = 50pF; V_{CC} = 5V$	3.2 3.1	ns
C _{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	4	pF
C _{I/O}	I/O pin capacitance	V _O = 0V or V _{CC} ; 3-State	7	pF
I _{CCZ}	Total supply current	Outputs disabled; V _{CC} = 5.5V	65	μΑ

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52-pin plastic Quad Flat Pack	-40°C to +85°C	MB2245 BB	MB2245 BB	SOT379-1

PIN CONFIGURATION



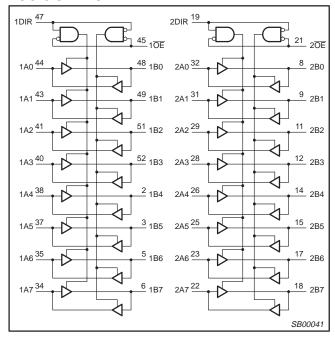
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 19	1DIR, 2DIR	Direction control inputs (Active-High)
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1B0 – 1B7, 2B0 – 2B7	Data outputs/outputs (B side)
45, 21	1 OE , 2 OE	Output enable (Active-Low)
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V _{CC}	Positive supply voltage

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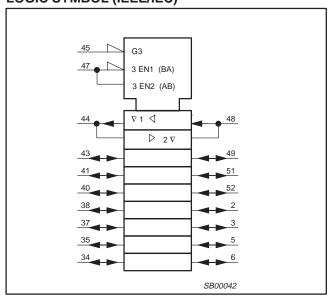
LOGIC SYMBOL

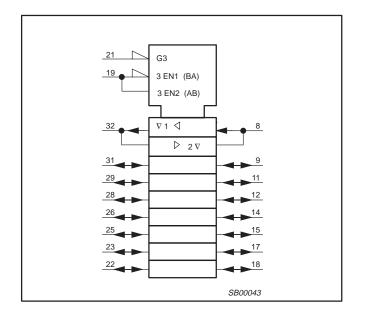


FUNCTION TABLE

INP	UTS	INPUTS/C	OUTPUTS
nOE	nDIR	nAx	nBx
L	L	A = B	Inputs
L	Н	Inputs	B = A
Н	Х	Z	Z

LOGIC SYMBOL (IEEE/IEC)





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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
VI	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIM	UNIT	
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
VI	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the
device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to
absolute-maximum-rated conditions for extended periods may affect device reliability.

^{2.} The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

^{3.} The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

					LIMITS			
SYMBOL PARAMETER		TEST CONDITIONS	Ta	_{mb} = +25	s∘C		-40°C 85°C	UNIT
			Min	Тур	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
		$V_{CC} = 4.5V$; $I_{OH} = -3mA$; $V_I = V_{IL}$ or V_{IH}	2.5	2.9		2.5		V
V _{OH}	High-level output voltage	$V_{CC} = 5.0V$; $I_{OH} = -3mA$; $V_I = V_{IL}$ or V_{IH}	3.0	3.4		3.0		V
		$V_{CC} = 4.5V$; $I_{OH} = -32mA$; $V_I = V_{IL}$ or V_{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	$V_{CC} = 4.5V$; $I_{OL} = 64mA$; $V_I = V_{IL}$ or V_{IH}		0.42	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μΑ
I _{OFF}	Power-off leakage current	$V_{CC} = 0.0V$; V_O or $V_I \le 4.5V$		±5.0	±100		±100	μΑ
I _{PU} /I _{PU}	Power-up/down 3-State output current	$V_{\underline{CC}}$ = 2.0V; $V_{\underline{O}}$ = 0.5V; $V_{\underline{I}}$ = GND or $V_{\underline{CC}}$; $V_{\underline{OE}}$ = $V_{\underline{CC}}$		±5.0	±50		±50	μА
I _{OZH}	3-State output High current	$V_{CC} = 5.5V; V_{O} = 2.7V; V_{I} = V_{IL} \text{ or } V_{IH}$		5.0	50		50	μΑ
l _{OZL}	3-State output Low current	$V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} \text{ or } V_{IH}$		-5.0	-50		-50	μΑ
I _{CEX}	Output high leakage current	$V_{CC} = 5.5V$; $V_{O} = 5.5V$; $V_{I} = GND$ or V_{CC}		5.0	50		50	μΑ
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-70	-180	-50	-180	mA
I _{CCH}		$V_{CC} = 5.5V$; Outputs High, $V_{I} = GND$ or V_{CC}		65	250		250	μΑ
Iccl	Quiescent supply current	$V_{CC} = 5.5V$; Outputs Low, $V_I = GND$ or V_{CC}		48	60		60	mA
I _{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_{I} = GND or V_{CC}		65	250		250	μА
Δl _{CC}	Additional supply current per input pin ²	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
 This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500 Ω

					LIMIT	S		
SYMBOL	PARAMETER	WAVEFORM	T _e	_{amb} = +25° CC = +5.0°	C V	T _{amb} = -40° V _{CC} = +5.	°C to +85°C .0V ±0.5V	UNIT
			Min	Тур	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.2 1.2	3.2 3.1	4.5 4.5	1.2 1.2	5.1 5.1	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	2.1 2.4	3.8 4.7	5.2 6.1	2.1 2.4	5.8 7.1	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	2.1 2.1	4.5 4.0	5.8 5.3	2.1 2.1	6.4 5.9	ns

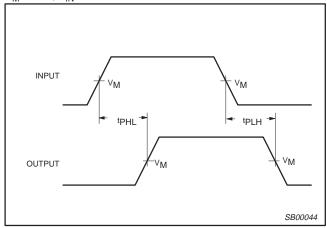
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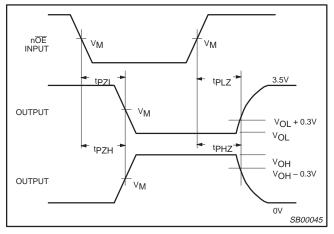
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AC WAVEFORMS

 $V_{M} = 1.5V, V_{IN} = GND \text{ to } 3.0V$

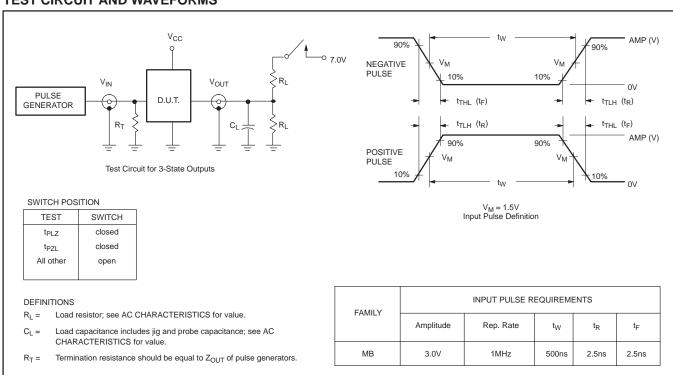


Waveform 1. Waveforms Showing the Input to Output Propagation Delays



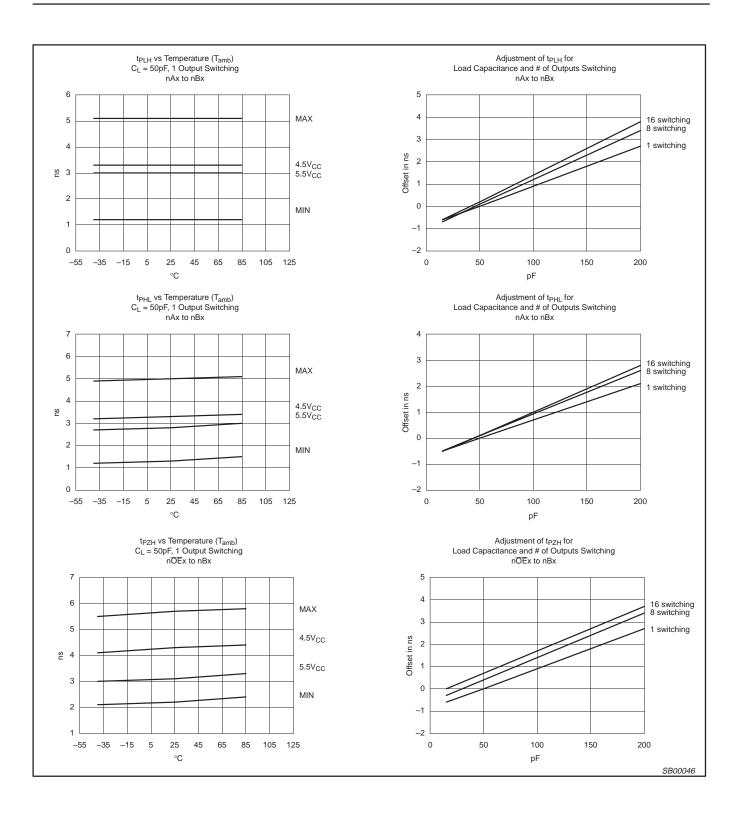
Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



16-bit transceiver with direction pins (3-State)

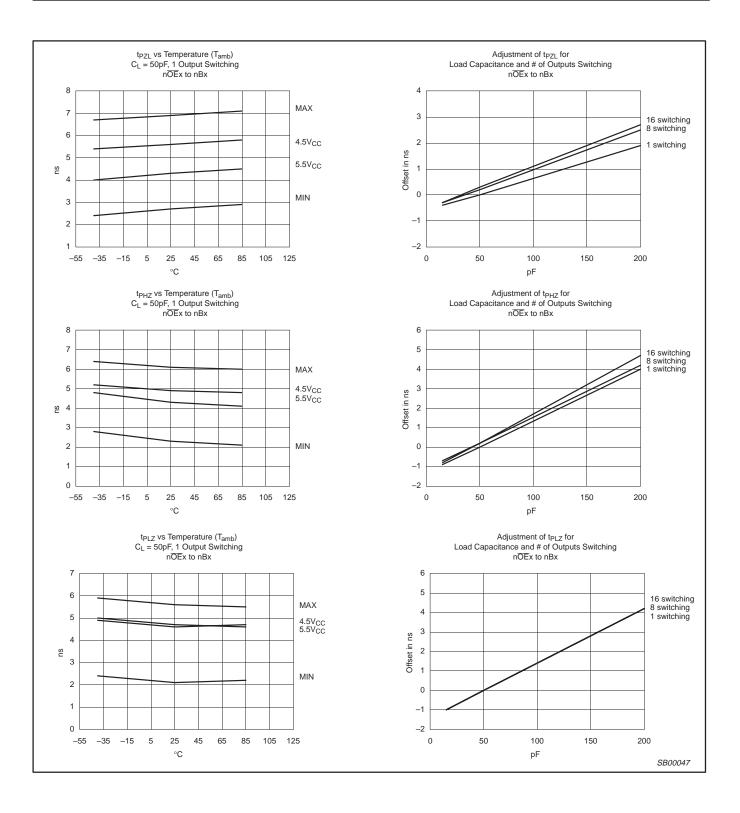
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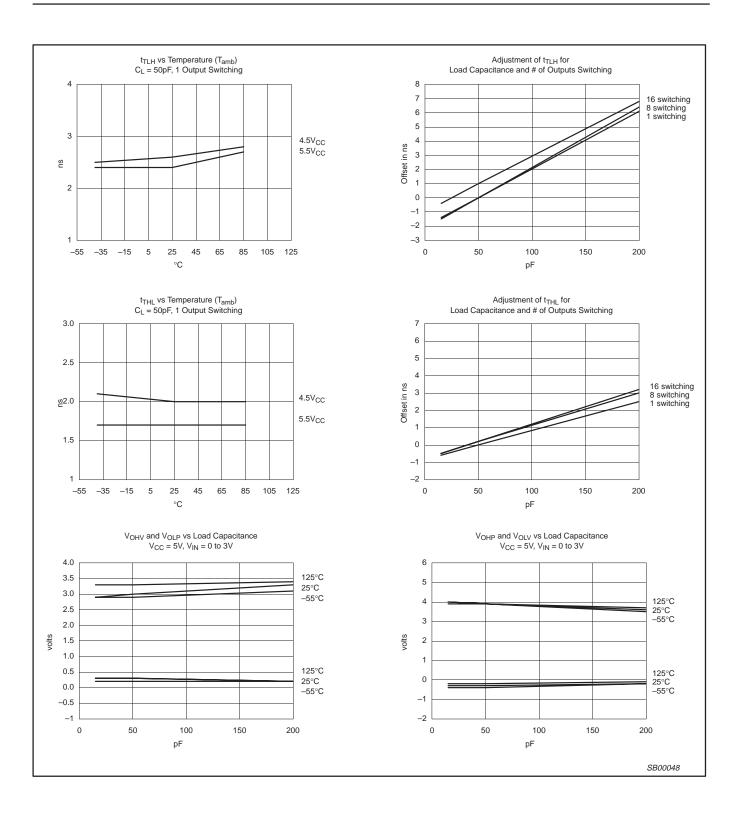
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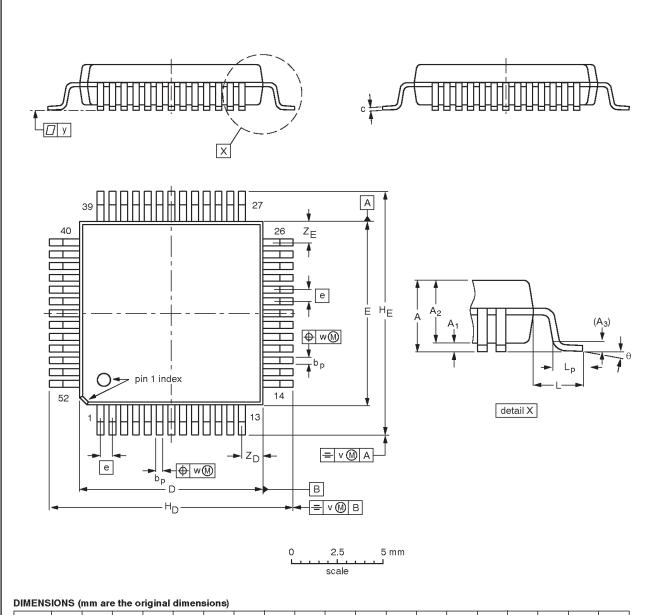


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QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm

SOT379-1



UNIT	A max.	A ₁	A ₂	Α3	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	H _D	HE	L	Lp	v	w	у	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
SOT379-1		MO-108			-95-02-04- 97-08-04

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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^[1] Please consult the most recently issued datasheet before initiating or completing a design.

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