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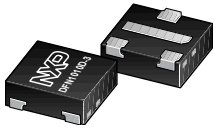
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Kind regards,

Team Nexperia



PBSS5160QA

60 V, 1 A PNP low V_{CEsat} (BISS) transistor

23 August 2013

Product data sheet

1. General description

PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

NPN complement: PBSS4160QA.

2. Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- High energy efficiency due to less heat generation
- Reduced Printed-Circuit Board (PCB) area requirements
- Solderable side pads
- AEC-Q101 qualified

3. Applications

- Loadswitch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

4. Quick reference data

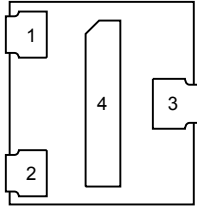
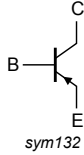
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-60	V
I_C	collector current		-	-	-1	A
I_{CM}	peak collector current	$t_p \leq 1$ ms; pulsed	-	-	-1.5	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1$ A; $I_B = -100$ mA; pulsed; $t_p \leq 300$ μ s; $\delta \leq 0.02$; $T_{amb} = 25$ °C	-	225	330	m Ω



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 <p>Transparent top view DFN1010D-3 (SOT1215)</p>	
2	E	emitter		
3	C	collector		
4	C	collector		

6. Ordering information

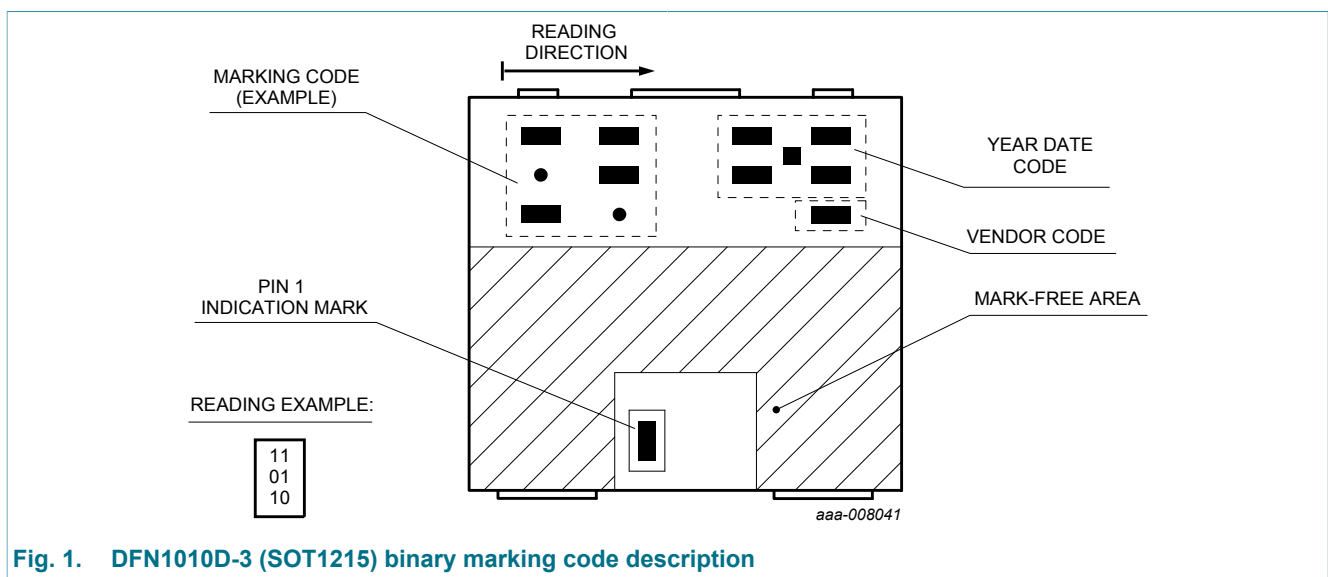
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS5160QA	DFN1010D-3	plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS5160QA	10 10 10



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-60	V
V_{CEO}	collector-emitter voltage	open base		-	-60	V
V_{EBO}	emitter-base voltage	open collector		-	-7	V
I_C	collector current			-	-1	A
I_{CM}	peak collector current	$t_p \leq 1$ ms; pulsed		-	-1.5	A
I_B	base current			-	-0.3	A
I_{BM}	peak base current	$t_p \leq 1$ ms; pulsed		-	-1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	325	mW
			[2]	-	600	mW
			[3]	-	740	mW
			[4]	-	540	mW
			[5]	-	1000	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

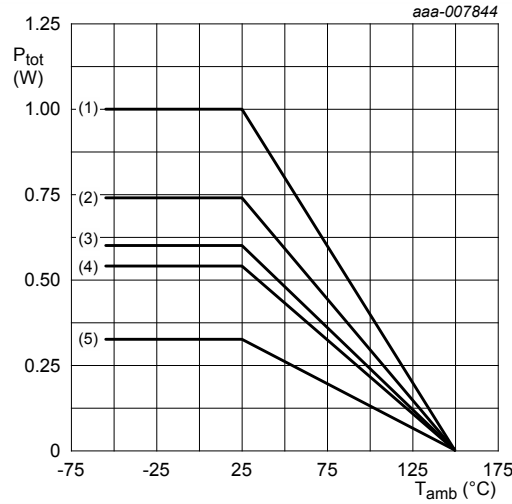
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 1 cm².

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 6 cm².

[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

[5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated mounting pad for collector 1 cm².



- (1) FR4 PCB, 4-layer copper, 1 cm²
- (2) FR4 PCB, single-sided copper, 6 cm²
- (3) FR4 PCB, single-sided copper, 1 cm²
- (4) FR4 PCB, 4-layer copper, standard footprint
- (5) FR4 PCB, single-sided copper, standard footprint

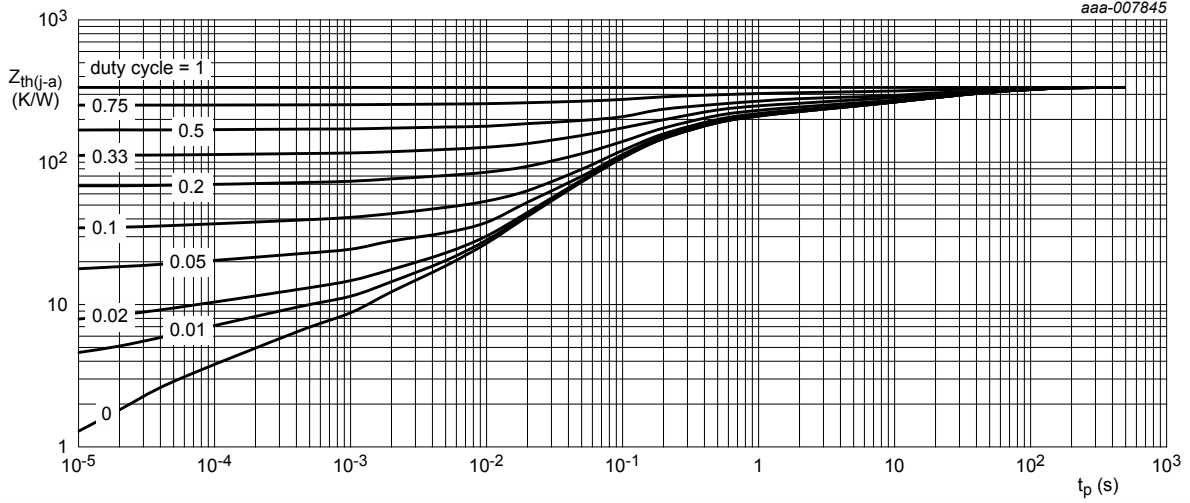
Fig. 2. Power derating curves

9. Thermal characteristics

Table 6. Thermal characteristics

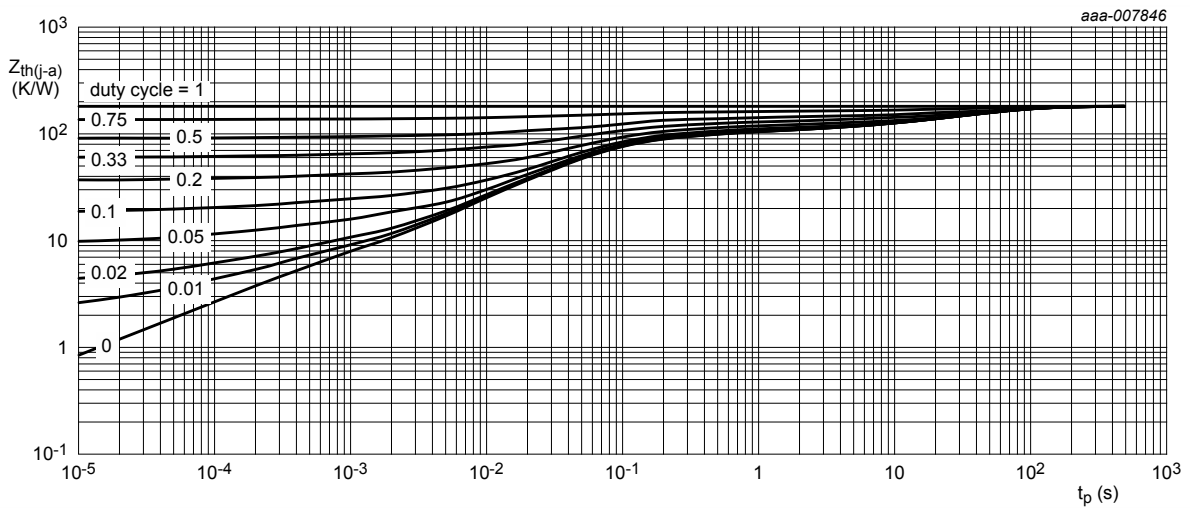
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
			[2]	-	-	209	K/W
			[3]	-	-	169	K/W
			[4]	-	-	232	K/W
			[5]	-	-	125	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 6 cm².
- [4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated mounting pad for collector 1 cm².



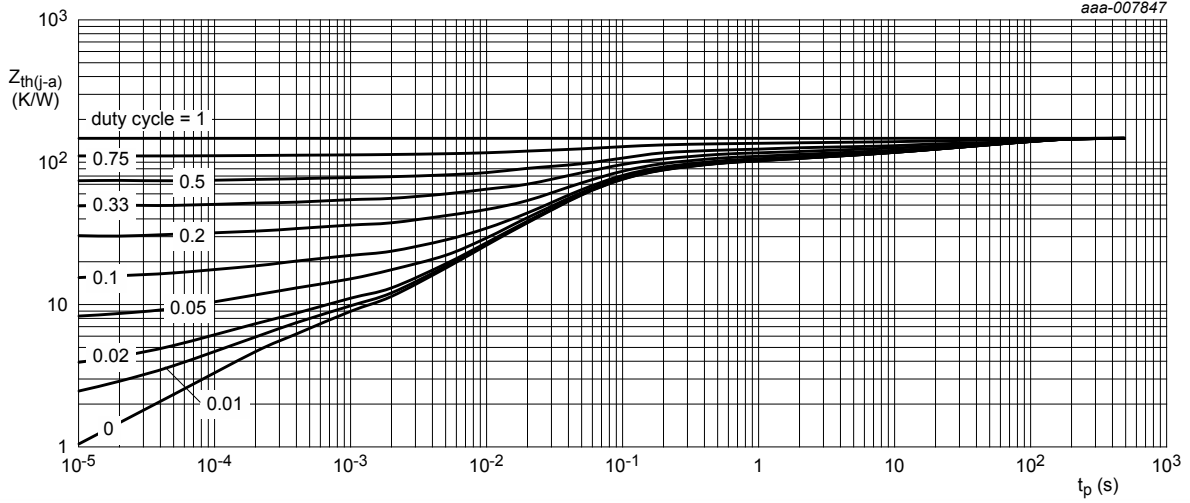
FR4 PCB, single-sided copper, standard footprint

Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



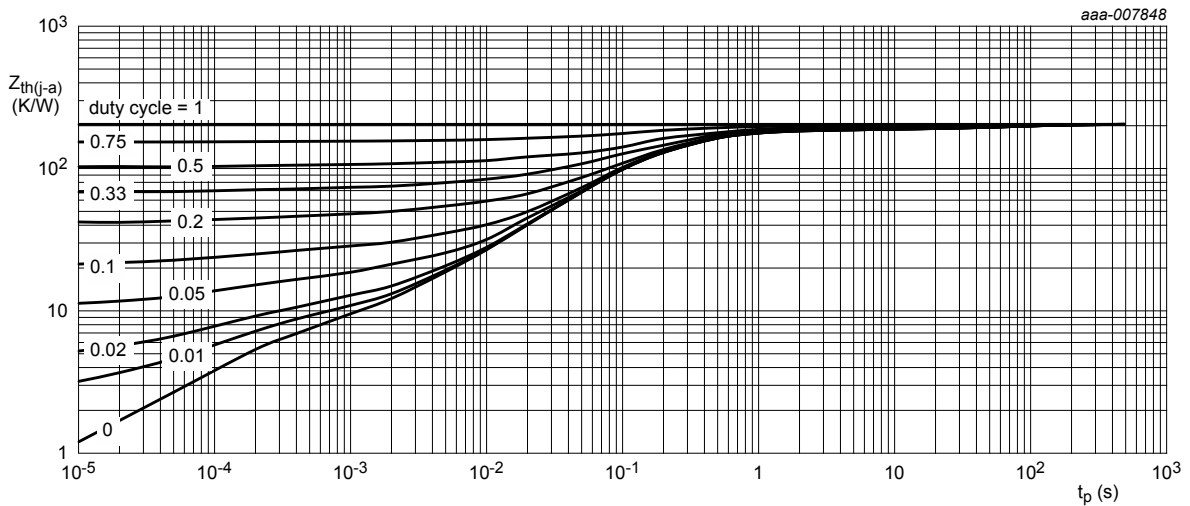
FR4 PCB, single-sided copper, 1 cm^2

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



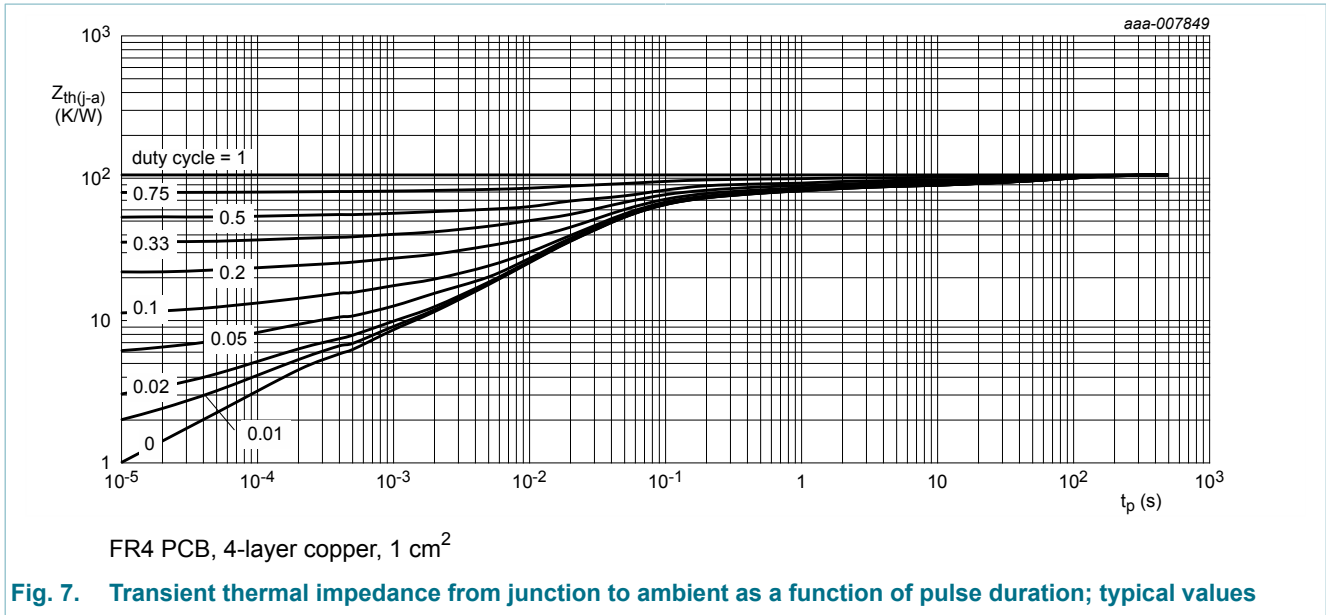
FR4 PCB, single-sided copper, 6 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, standard footprint

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

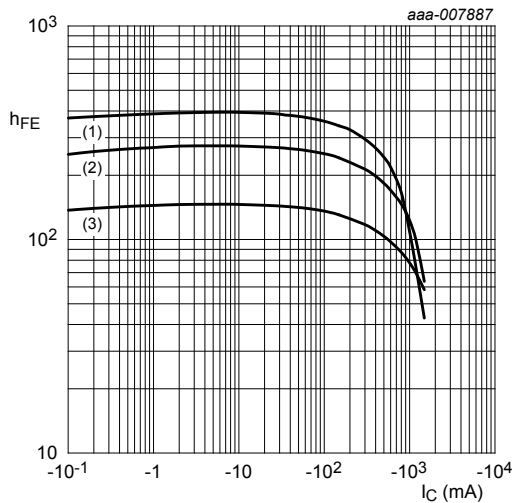


10. Characteristics

Table 7. Characteristics

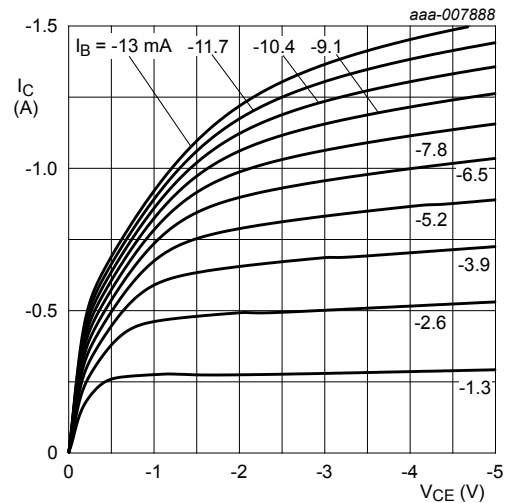
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CBO}	collector-base cut-off current	V _{CB} = -48 V; I _E = 0 A; T _{amb} = 25 °C	-	-	-100	nA
		V _{CB} = -48 V; I _E = 0 A; T _j = 150 °C	-	-	-50	μA
I _{CES}	collector-emitter cut-off current	V _{CE} = -48 V; V _{BE} = 0 V; T _{amb} = 25 °C	-	-	-100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -2 V; I _C = -100 mA; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C; pulsed	160	250	-	
		V _{CE} = -2 V; I _C = -500 mA; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C; pulsed	120	185	-	
		V _{CE} = -2 V; I _C = -1 A; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C; pulsed	85	125	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -500 mA; I _B = -50 mA; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-125	-190	mV
		I _C = -1 A; I _B = -50 mA; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-315	-460	mV
		I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-225	-330	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	225	330	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{BEsat}	base-emitter saturation voltage	I _C = -500 mA; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.88	-1	V
		I _C = -1 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.94	-1.05	V
		I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.97	-1.1	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = -2 V; I _C = -0.5 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.8	-0.9	V
t _d	delay time	V _{CC} = -10 V; I _C = -0.5 A; I _{Bon} = -25 mA; I _{Boff} = 25 mA; T _{amb} = 25 °C	-	15	-	ns
t _r	rise time		-	35	-	ns
t _{on}	turn-on time		-	50	-	ns
t _s	storage time		-	300	-	ns
t _f	fall time		-	50	-	ns
t _{off}	turn-off time		-	350	-	ns
f _T	transition frequency	V _{CE} = -10 V; I _C = -50 mA; f = 100 MHz; T _{amb} = 25 °C	100	150	-	MHz
C _c	collector capacitance	V _{CB} = -10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C	-	12	15	pF



V_{CE} = -2 V
 (1) T_{amb} = 100 °C
 (2) T_{amb} = 25 °C
 (3) T_{amb} = -55 °C

Fig. 8. DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

Fig. 9. Collector current as a function of collector-emitter voltage; typical values

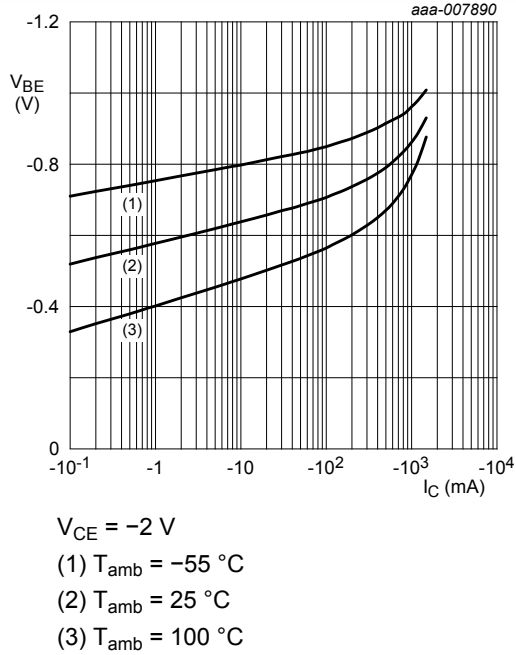


Fig. 10. Base-emitter voltage as a function of collector current; typical values

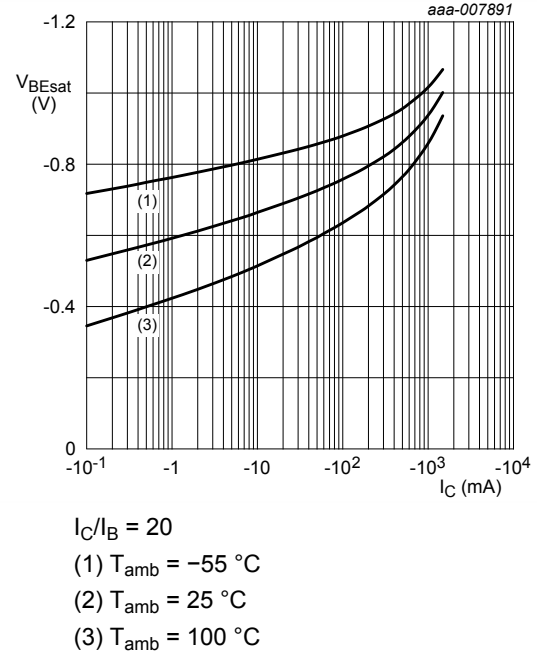


Fig. 11. Base-emitter saturation voltage as a function of collector current; typical values

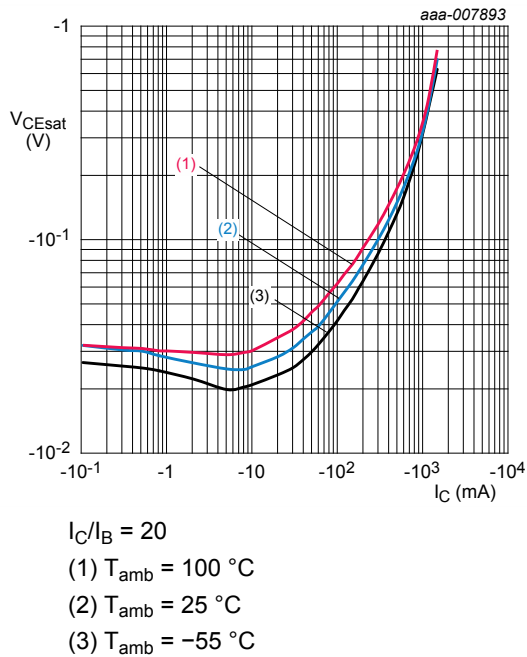


Fig. 12. Collector-emitter saturation voltage as a function of collector current; typical values

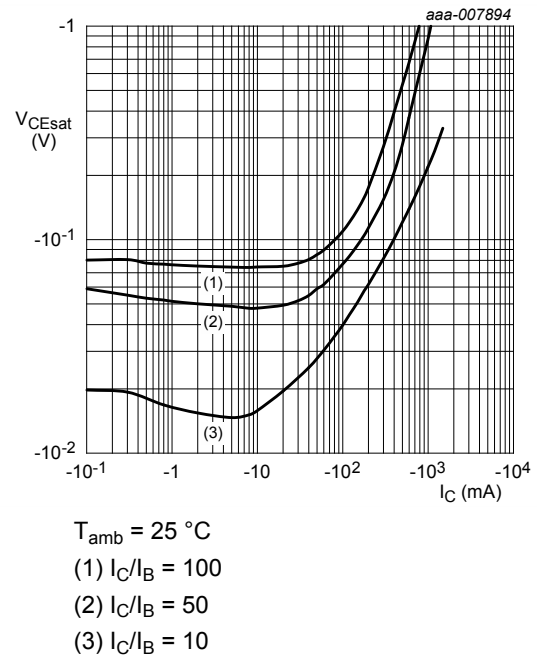
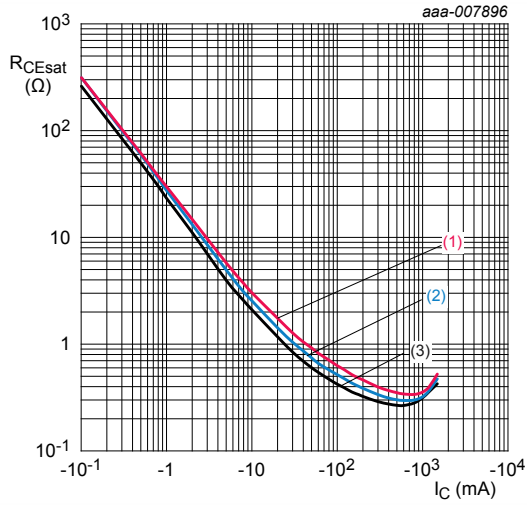
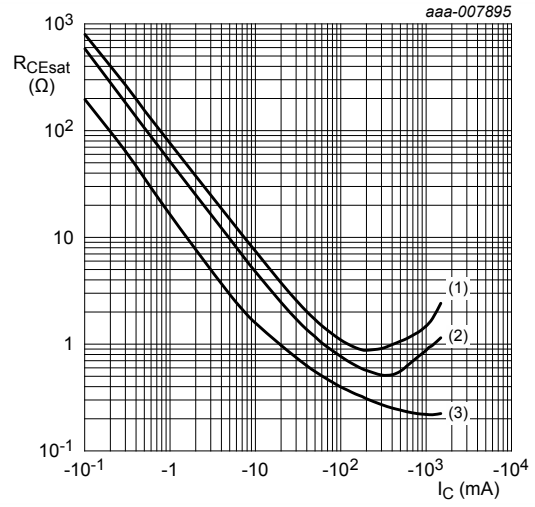


Fig. 13. Collector-emitter saturation voltage as a function of collector current; typical values



- $I_C/I_B = 20$
 (1) $T_{amb} = 100^\circ C$
 (2) $T_{amb} = 25^\circ C$
 (3) $T_{amb} = -55^\circ C$

Fig. 14. Collector-emitter saturation resistance as a function of collector current; typical values



- $T_{amb} = 25^\circ C$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig. 15. Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

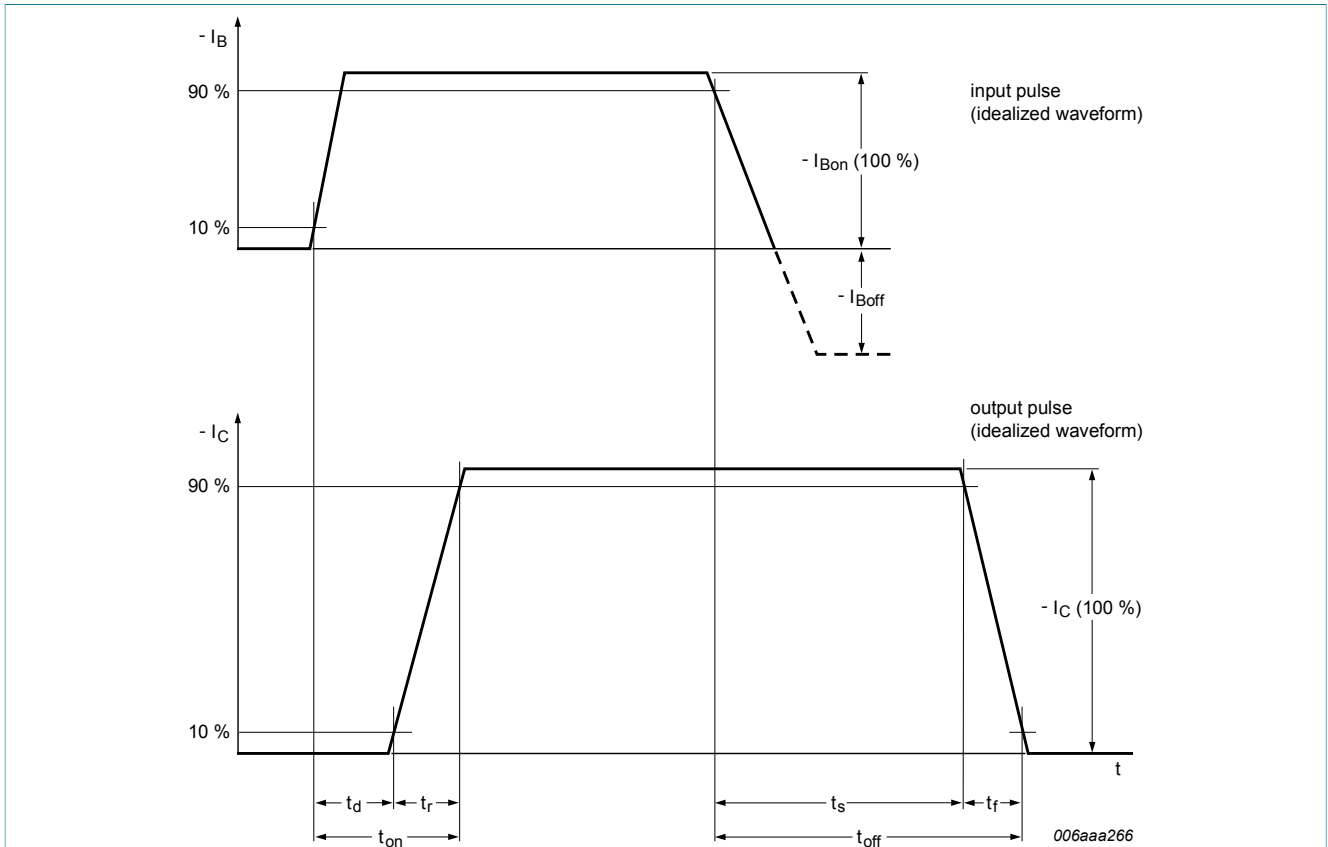


Fig. 16. BISS transistor switching time definition

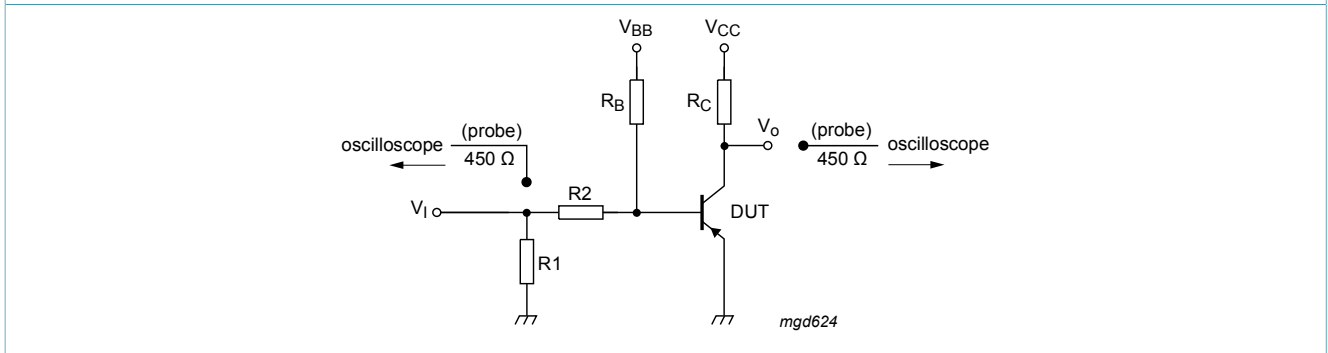


Fig. 17. Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

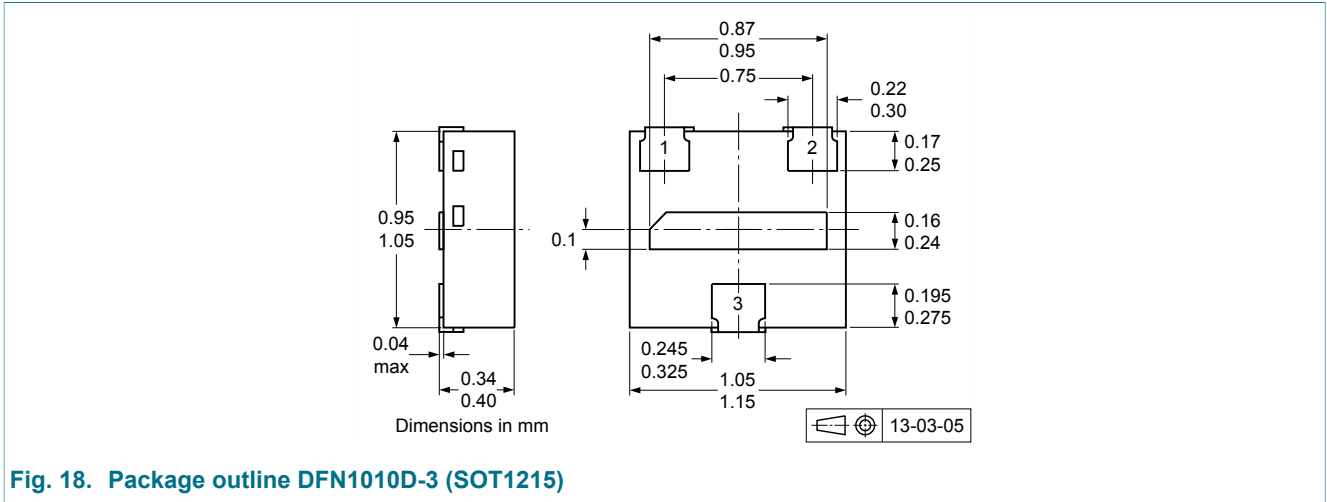


Fig. 18. Package outline DFN1010D-3 (SOT1215)

13. Soldering

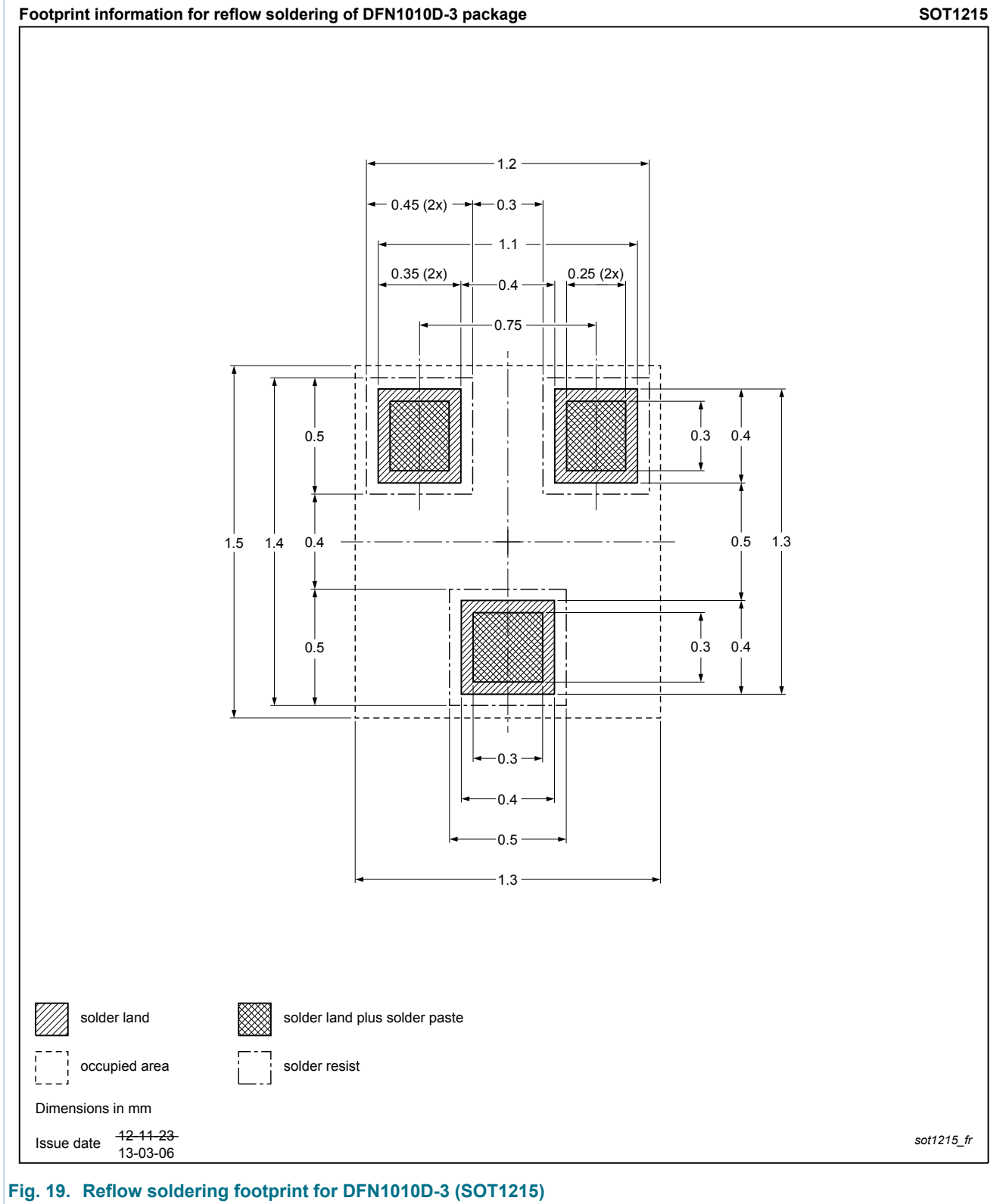


Fig. 19. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5160QA v.1	20130823	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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16. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	3
9	Thermal characteristics	4
10	Characteristics	7
11	Test information	11
11.1	Quality information	11
12	Package outline	12
13	Soldering	13
14	Revision history	14
15	Legal information	15
15.1	Data sheet status	15
15.2	Definitions	15
15.3	Disclaimers	15
15.4	Trademarks	16

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 Date of release: 23 August 2013
