Demonstration Board EPC9101 Quick Start Guide

EPC2014 + EPC2015 1 MHz Buck Converter

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9101 demonstration board is a 1.2 V output, 1 MHz buck converter with an 18 A maximum output current and 8 V to 19 V input voltage range. The demonstration board features the EPC2014 and EPC2015 enhancement mode field effect transistors (*eGaN*® FETs), as well as the first *eGaN* FET specific integrated circuit gate driver – the Texas Instruments LM5113. The EPC9101 board is not intended as a reference design, but to showcase the performance that can be achieved using the *eGaN* FETs and *eGaN* gate driver together.

The EPC9101 demonstration board is 3″ square and contains a fully closed loop buck converter.

There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1. For more information on the EPC2014/5 *eGaN* FETs or LM5113 driver, please refer to the datasheet available from EPC at www.epc-co.com and www.TI.com. These datasheets, as well that of the LT3833 controller should be read in conjunction with this quick start guide.

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Bus Input Voltage Range		8		19	V
V_{OUT}	Switch Node Output Voltage			1.2		V
I_{OUT}	Switch Node Output Current				18*	A
f_{SW}	Switching frequency			1000		kHz
	Peak Efficiency	12 V_{IN}, I_{OUT} = 9 A		88		%
	Full Load Efficiency	12 V_{IN}, I_{OUT} = 18 A		85		%
	Full Load Efficiency	19 V_{IN}, I_{OUT} = 17 A		84		%

*Maximum limited by thermal considerations

Quick Start Procedure

The demonstration board EPC9101 is easy to set up to evaluate the performance of the EPC2014 and EPC2015 eGaN FETs and LM5113 gate driver. Refer to Figure 2 for proper connection and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus between V_{IN} and GND banana jacks as shown.
2. With power off, connect the active (constant current) load as desired between V_{OUT} and GND banana jacks as shown.
3. Turn on the supply voltage to the required value (do not exceed the absolute maximum voltage of 19 V on V_{IN}).
4. Measure the output voltage to make sure the board is fully functional and operating no-load.
5. Turn on active load to the desired load current while staying below the maximum current (< 17 A or < 18 A depending on input)
6. Once operational, adjust the bus voltage and load current within the allowed operating range and observe the output switching behavior, efficiency and other parameters.
7. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node of the gate voltage, care must be taken to avoid long ground leads. Measure these by placing the oscilloscope probe tip through the large vias provided and grounding the probe directly across the GND vias provided. See Figure 3 for proper scope probe conection technique. Scope jacks can be soldered onto the board at these locations as desired.

NOTE. The dead-times for both the leading and trailing edges have been adjusted for optimum full load efficiency. Further adjustment is not recommended, but can be done at one's own risk. This should be done while monitoring both the input current and switch-node voltage to determine the effect of these adjustments. Under no circumstance should the input pins to the LM5113 be probed during operation as the added probe capacitance will alter the device timing.

CIRCUIT PERFORMANCE

The EPC9101 demonstration circuit was designed to showcase the size and performance that can readily be achieved at 1 MHz operation using *eGaN* FETs. To ensure 19 V_{IN} operation, the *eGaN* FETs' switching transitions have been increased to ensure operation within the device limits. Alternative methods such as snubbers, voltages clamps etc., are also possible by utilizing the optional footprints provided.

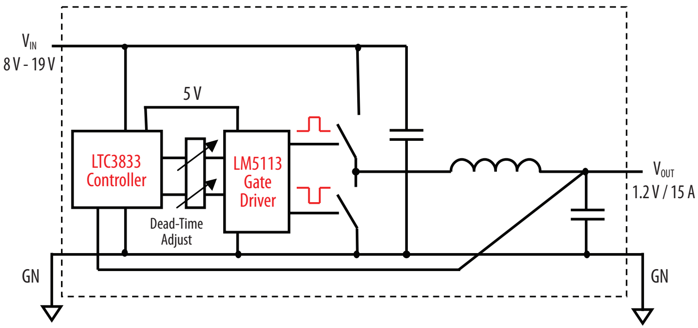


Figure 1: Block Diagram of EPC9101 Demonstration Board

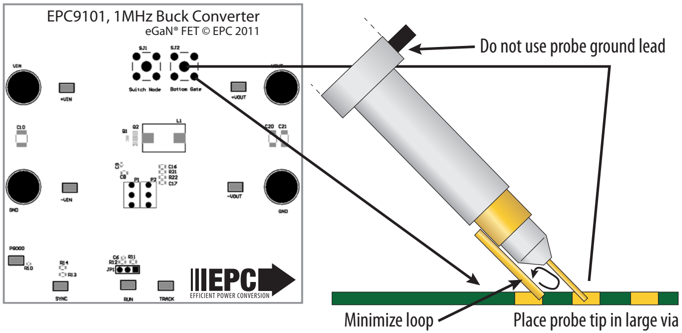


Figure 3: Proper Measurement of Switch Node or Gate Voltage

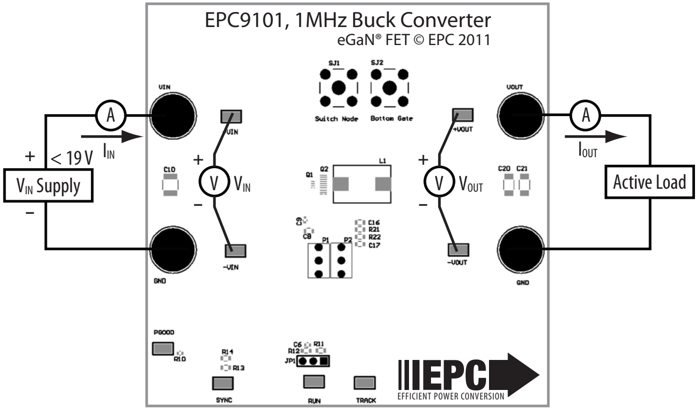


Figure 2: Proper Connection and Measurement Setup

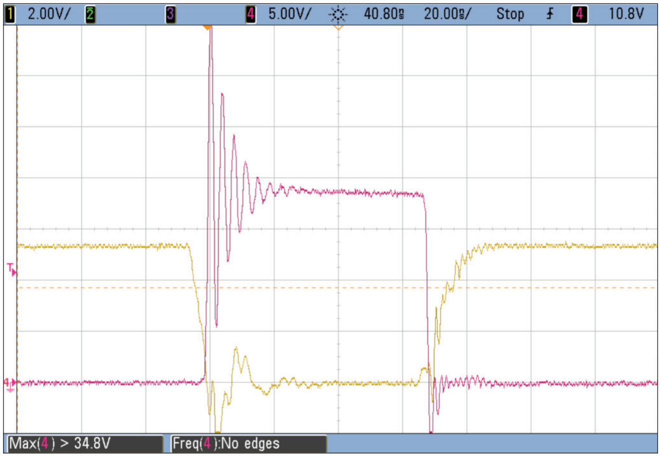


Figure 4: Typical waveforms for a 19 V to 1.2 V/15 A (1 MHz) Buck converter
CH1: Low side gate voltage – CH4: Switch node voltage

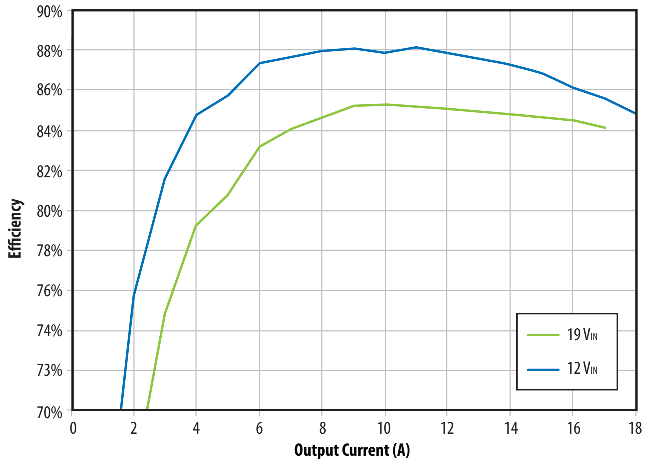
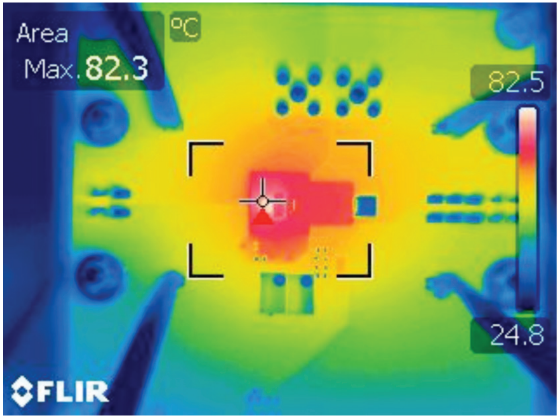


Figure 5: Typical efficiency curves for 19 V and 12 V input

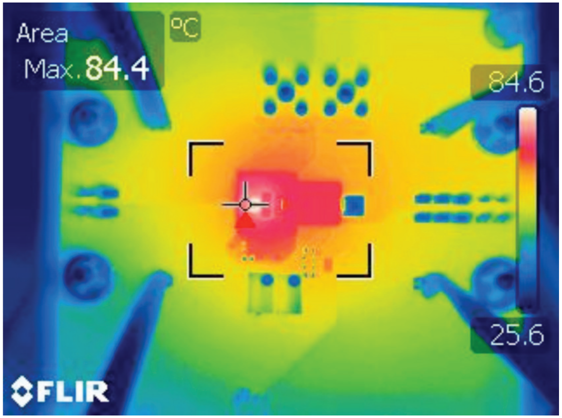
THERMAL CONSIDERATIONS

The EPC9101 demonstration board thermal images for steady state full load operation are shown in Figure 6. The EPC9101 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling could increase the current capability of the demonstration circuit, but care must be taken to not exceed the absolute maximum die temperature of 125°C and stay within the constraints of the other components within the circuit.

NOTE. The EPC9101 demonstration board does not have any current or thermal protection on board.



12 VIN, 18 AOUT

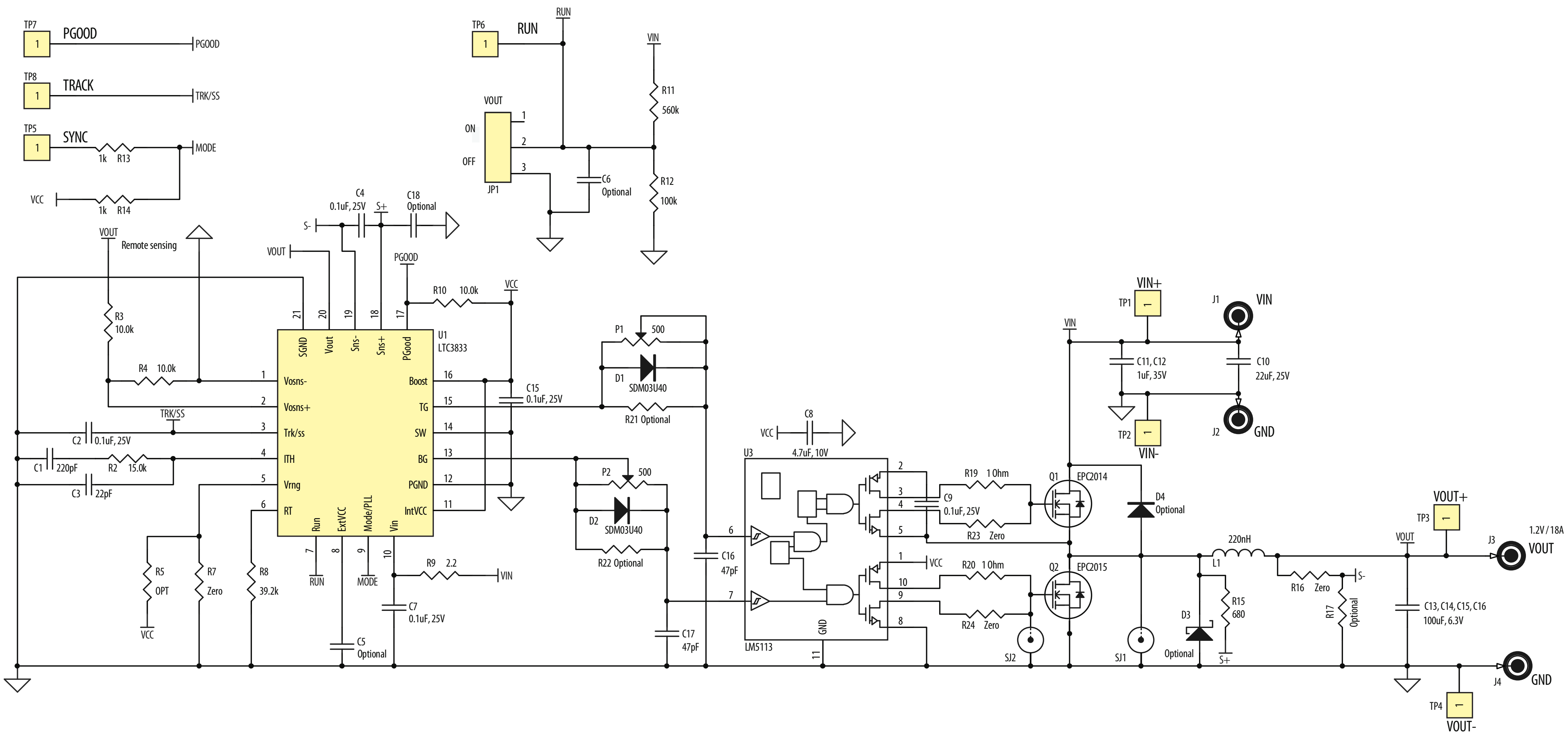


19 VIN, 17 AOUT

Figure 6: Thermal images of EPC9101 under full load conditions

Table 2 : Bill of Material

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	1	C1	Capacitor, 220pF, 5%, 50V, NP0	Murata, GRM1885C1H221JA01D
2	1	C3	Capacitor, 22pF, 5%, 50V, NP0	Murata, GRM1885C1H220JA01D
3	5	C2, C4, C7, C9, C15	Capacitor, 0.1uF, 10%, 25V, X5R	TDK, C1005X5R1E104K
4	1	C8	Capacitor, 4.7uF, 10%, 10V, X5R	TDK, C1608X5R1A475K
5	1	C10	Capacitor, 22uF, 20%, 25V, X5R	Taiyo Yuden, TMK325BJ226MM
6	2	C11, C12	Capacitor, 1uF, 10%, 35V, X7R	Murata, GCM21BR7YA105KA55L
7	4	C13, C14, C20, C21	Capacitor, 100uF, 20%, 6.3V, X5R	TDK, C3216X5R0J107M
8	2	C16, C17	Capacitor, 47PuF, 5%, 50V, NP0	TDK, C1608C0G1H470J
9	2	D1, D2	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
10	4	J1, J2, J3, J4	Banana Jack	Keystone, 575-4
11	1	JP1	Connector	3pins of Tyco, 4-103185-0
12	1	L1	Inductor, 0.22uH, 30A	Wurth, 744303022
13	2	P1, P2	Potentiometer, 500 Ohm, 0.25W	Murata, PV37Y501C01B00
14	1	Q1	eGaN® FET	EPC, EPC2014
15	1	Q2	eGaN® FET	EPC, EPC2015
16	1	R2	Resistor, 15.0K, 1%, 1/8W	Stackpole, RMCF0603FT15K0
17	1	R3	Resistor, 10.0K, 1%, 1/8W	Stackpole, RMCF0603FT10K0
18	2	R4, R10	Resistor, 10.0K, 1%, 1/10W	Panasonic, ERJ-2RKF1002X
19	3	R7, R23, R24	Resistor, 0 Ohm, 1/16W	Stackpole, RMCF0402ZT0R00
20	1	R8	Resistor, 39.2K, 1%, 1/8W	Stackpole, RMCF0603FT39K2
21	1	R9	Resistor, 2.2 Ohm, 5%, 1/16W	Yageo, RC0402FR-072R2L
22	1	R11	Resistor, 560K, 1%, 1/8W	Stackpole, RMCF0603FT560K
23	1	R12	Resistor, 100K, 1%, 1/8W	Stackpole, RMCF0603FT100K
24	2	R13, R14	Resistor, 1.00K, 5%, 1/10W	Rohm, MCR03EZPJ102
25	1	R15	Resistor, 680 Ohm, 5%, 1/8W	Stackpole, RMCF0603FT680R
26	1	R16	Resistor, 0 Ohm, 1/8W	Stackpole, RMCF0603FT00R0
27	2	R19, R20	Resistor, 1 Ohm, 5%, 1/16W	Yageo, RC0402JR-071RL
28	8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Measurement Point	Keystone Elect, 5015
29	1	U1	I.C., Buck Regulator	Linear Technology, LTC3833EUDC#PBF
30	1	U2	I.C., Gate driver	Texas Instruments, LM5113
31	4		Nylon Stand-offs	Keystone, 8834
32	0	XJP1	Optional Jumper	
33	0	R5, R17, R21, R22	Optional Resistors	
34	0	C5, C6, C18	Optional Capacitors	
35	0	SJ1, SJ2	Optional Scope Jack	Example: Tektronix 131-5031-00
36	0	D3	Optional Diode	
36	0	D4	Optional Diode	



Demonstration Board – EPC9101 Schematic

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