

## PIC18F1230/1330 Rev. B0 Silicon Errata

The PIC18F1230/1330 Rev. B0 parts you have received conform functionally to the Device Data Sheet (DS39758C), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F1230/1330 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

**The following silicon errata apply only to PIC18F1230/1330 devices with these Device/Revision IDs:**

Part Number	Device ID	Revision ID
PIC18F1230	0001 1110 000	0 0110
PIC18F1330	0001 1110 001	0 0110

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F1230/1330 silicon.

### 1. Module: Comparator

The CMPxIF flag, which indicates when each comparator has a switched state, cannot be cleared immediately after reading CMCON. The mismatch condition that sets CMPxIF persists for 1 Tcy after reading/writing CMCON.

#### Work around

Insert a NOP instruction between reading/writing CMCON and clearing the CMPxIF flag.

#### Date Codes that pertain to this issue:

All engineering and production devices.

### 2. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations, one or more extra bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted – only extra bytes are added. The extra bytes may be 0x00 or 0xFF.

This situation occurs when the contents of the transmit buffer (TXREG) are transferred to the TSR at the end of the Stop bit period at the same time that firmware writes to TXREG.

Note that TXIF is set at the beginning of the Stop bit period.

#### Work around

None.

#### Date Codes that pertain to this issue:

All engineering and production devices.

### 3. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTA <7> = 0)
- The EUSART is re-enabled (RCSTA <7> = 1)
- A two-cycle instruction is executed

#### Work around

Add a 2 Tcy delay after re-enabling the EUSART.

1. Disable receive interrupts (RCIE bit, PIE1<5> = 0).
2. Disable the EUSART (RCSTA <7> = 0).
3. Re-enable the EUSART (RCSTA <7> = 1).
4. Re-enable receive interrupts (PIE1<5> = 1).  
(This is the first Tcy delay.)
5. Execute a NOP instruction.  
(This is the second Tcy delay.)

#### Date Codes that pertain to this issue:

All engineering and production devices.

# PIC18F1230/1330

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## REVISION HISTORY

Rev A Document (12/2008)

Initial release of this errata. Includes silicon issues 1 (Comparator) and 2-3 (Enhanced Universal Synchronous Asynchronous Receiver Transmitter – EUSART).

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