Wideband, Dual Rx Mixers with Integrated IF Amplifiers

Data Sheet

ADRF6658

FEATURES

- Wideband, dual-channel, active downconversion mixers
- Low distortion, fast settling, IF DGAs
- RF input frequency range: 690 MHz to 3.8 GHz
- Programmable baluns on RF inputs
- For RF = 1950 MHz, IF = 281 MHz, high linearity mode
  - Voltage conversion gain, including IF filter loss: −5 dB to +26.5 dB
  - Input IP3: 29 dBm at minimum DGA gain
  - Input P1dB: 12 dBm at minimum DGA gain
  - SSB NF: 13 dB at maximum DGA gain
  - Output IP3: 40 dBm at maximum DGA gain
  - Output P1dB: 19 dBm at maximum DGA gain
  - Channel isolation: 52 dB
- Differential and single-ended LO input modes
- Differential IF output impedance: 100 Ω
- Flexible power-down modes for low power operation
  - Power-up time after enabling channels: 100 ns, typical
- Programmable via a 3-wire serial port interface (SPI)
- Single 3.3 V supply
  - High linearity mode: 440 mA
  - Low power mode: 260 mA

APPLICATIONS

- Cellular base stations and wireless infrastructure receivers (W-CDMA, TD-SCDMA, WiMAX, GSM, LTE, PCS, DCS, DECT)
- Active antenna systems
- PTP radio link down converters
- Wireless LANs and CATV equipment

GENERAL DESCRIPTION

The ADRF6658 is a high performance, low power, wideband, dual-channel radio frequency (RF) downconverter with integrated intermediate frequency (IF) digitally controlled amplifiers (DGAs) for wideband, low distortion base station radio receivers.

The dual Rx mixers are doubly balanced Gilbert cell mixers with high linearity and excellent image rejection. Both mixers convert 50 Ω RF inputs to open-collector broadband IF outputs. Internal tunable baluns on the RF inputs enable suppression of RF signal harmonics and attenuation of out-of-band signals before the mixer inputs, reducing input reflections and out-of-band interference signals. A flexible local oscillator (LO) architecture allows the use of differential or single-ended LO signals.

The dual-channel IF DGAs are based on the ADL5201 and ADL5202 and have a fixed, differential output impedance of 100 Ω. The gain is adjustable over a 31.5 dB range with a 0.5 dB step size via the on-chip SPI, or through independent, 6-bit parallel ports that support latch functionality. Each channel, from the mixer inputs to the IF amplifier outputs, together with an LC interstage band-pass filter, achieves a maximum voltage conversion gain of 26.5 dB.

Fabricated with the Analog Devices, Inc., high speed SiGe process, the ADRF6658 is available in a compact, 7 mm × 7 mm, 48-lead LFCSP package, and operates over the −40°C to +105°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

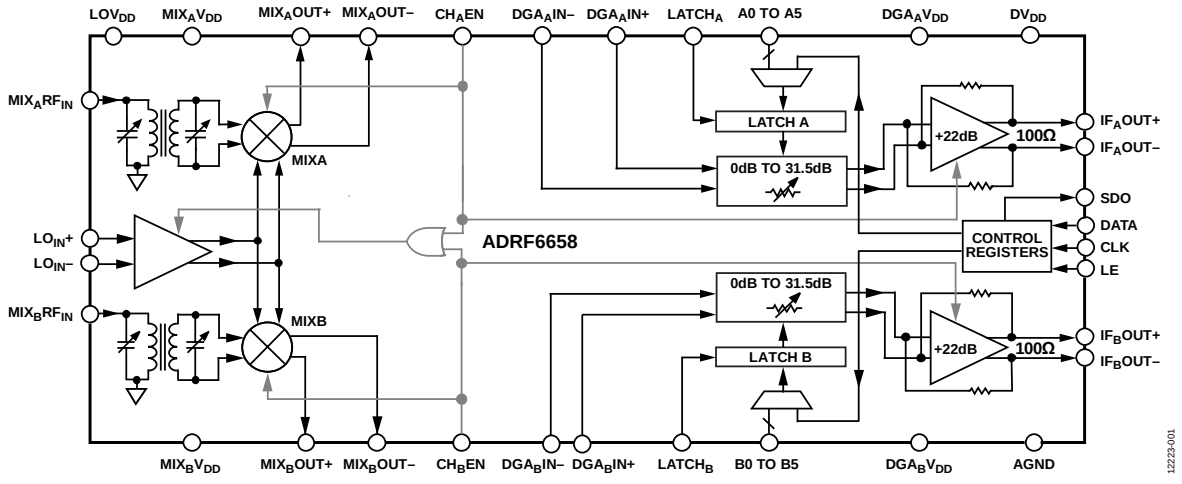

Figure 1.

Rev. A

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

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Data Sheet

- ADRF6658: Wideband, Dual Rx Mixers with Integrated IF Amplifiers

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- ADRF6658 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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1/15—Revision 0: Initial Version

SPECIFICATIONS

MIX_AV_{DD} = MIX_BV_{DD} = DV_{DD} = LOV_{DD} = DGA_AV_{DD} = DGA_BV_{DD} = 3.3 V ± 5%; AGND = 0 V. T_A = T_{MIN} to T_{MAX}. The operating temperature range = −40°C to +105°C. Parameters are measured on a standard test circuit with an IF filter; f_{RF} = 1.95 GHz, RF input power (P_{RF}) = −10 dBm, f_{LO} = 2.231 GHz, LO input power (P_{LO}) = 0 dBm, and f_{IF} = 281 MHz, using standard register settings. For IP2 and IP3 measurements, f_{RF1} = 1.949 GHz and f_{RF2} = 1.951 GHz, maximum DGA gain, high linearity mode, unless otherwise noted. R_{SOURCE} = 50 Ω, R_{LOAD} = 100 Ω, differential.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING CONDITIONS					
RF Input Frequency	690		3800	MHz	
LO Power Level	−6	0	+6	dBm	
LO Frequency	690		4100	MHz	
CHANNEL CHARACTERISTICS					
RF Input Return Loss		−12		dB	Register 13, Bits[DB12:DB7] programmed according to RF frequency
IF Output Return Loss		−10		dB	Within IF filter passband
IF Lower Cutoff Frequency[1]		10		MHz	f_{-3dB}, MIX_xOUT_y connected to DGA_xIN_y through a dc block capacitor
IF Upper Cutoff Frequency		520		MHz	f_{-3dB}, MIX_xOUT_y connected to DGA_xIN_y through a dc block capacitor
Voltage Conversion Gain		26.5		dB	Maximum DGA gain
Voltage Conversion Gain		−5		dB	Minimum DGA gain
Input P1dB					
High Linearity Mode		12		dBm	Register 13, Bits[DB24:DB22] = 4
Low Power Mode		4		dBm	Register 13, Bits[DB24:DB22] = 1
Second Order Input Intercept (IIP2)		49		dBm	P_{RF} = 0 dBm per tone, minimum DGA gain, high linearity mode
Third Order Input Intercept (IIP3)					P_{RF} = 0 dBm per tone, minimum DGA gain
High Linearity Mode		29		dBm	
Low Power Mode		17		dBm	
SSB NF					High linearity mode
RF = 855 MHz		12.8		dB	
RF = 1950 MHz		13		dB	
RF = 3795 MHz		14.4		dB	
With a 5 dBm Blocker		25		dB	
LO to RF Leakage		−30		dBm	
LO to IF Leakage		−40		dBm	
RF to IF Leakage		−50		dBc	Relative to IF output level
2 LO − 2 RF		−55		dBc	
3 LO − 3 RF		−55		dBc	
IF Output and LO Leakage Intermodulation Spur	−70	−100		dBc	f_{LO} = 3.249 GHz, f_{RF} = 3.5 GHz, IF DGA output power (P_{IFOUT}) = 9 dBm, f_{SPUR} = 237 MHz and 265 MHz
Channel Isolation		52		dB	f_{RF} = 1.95 GHz, f_{LO} = 2.231 GHz, maximum DGA gain
Mixer V to I Bias Adjustment Effects					Register 13, Bits[DB24:DB22] changing from 4 to 1
Amplitude Variation		0.19		dB	
Gain Step		0.5		dB	
Gain Conformance Error		0.05		dB	Any two adjacent steps
Phase Conformance Error		0.5		Degrees	Any two adjacent steps
Output P1dB		19		dBm	Maximum DGA gain
Output IP3		40		dBm	Maximum DGA gain
Differential Output Impedance		100		Ω	
Second Harmonic Level		−65		dBc	At 2 V p-p
Third Harmonic Level		−65		dBc	At 2 V p-p

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.17		3.6	V	
Input Low Voltage, V_{INL}	−0.5		+0.63	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}		2		pF	
LOGIC OUTPUTS					SDO (Pin 32)
Output High Voltage, V_{OH}	V_{LOGIC} − 0.4			V	V_{LOGIC} selected with Register 5, Bit DB24
Output High Current, I_{OH}			500	µA	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
DV_{DD}	3.15	3.3	3.45	V	
MIX_AV_{DD}, MIX_BV_{DD}, DGA_AV_{DD}, DGA_BV_{DD}, and LOV_{DD}		DV_{DD}			The voltages on these pins must equal DV_{DD}
External $IF_XOUT±$ Pull-Up Supply			DV_{DD}	V	
Mixer Current in High Linearity Mode		80		mA	Mixer V to I bias (Register 13, Bits[DB24:DB22]) = 4
Mixer Current in Low Power Mode		40		mA	Mixer V to I bias (Register 13, Bits[DB24:DB22]) = 1
IF DGA Current		140		mA	Per amplifier
Total Current					Dual Rx enabled
High Linearity Mode		440	550	mA	Mixer V to I bias (Register 13, Bits[DB24:DB22]) = 4
Low Power Mode		260		mA	Mixer V to I bias (Register 13, Bits[DB24:DB22]) = 1
Low Power Sleep Mode		450	1000	µA	
Standby Mode		65		mA	Both mixers and DGAs in standby mode
TIMING[2]					
Channel Power-Up from Standby Mode After Changing State of CH_AEN or CH_BEN		100	400	ns	From standby mode to normal operation

[1] DC-coupled; lower cutoff frequency determined mostly by external components.
[2] Not tested in production; guaranteed by characterization.

SUPPLEMENTAL INFORMATION FOR MIXERS AND IF DGAS

MIX_AV_{DD} = MIX_BV_{DD} = DV_{DD} = LOV_{DD} = DGA_AV_{DD} = DGA_BV_{DD} = 3.3 V ± 5%; AGND = 0 V. T_A = T_{MIN} to T_{MAX}. The operating temperature range = −40°C to +105°C. Parameters are measured on a standard test circuit with an IF filter; f_{RF} = 1.95 GHz, PRF = −10 dBm, f_{LO} = 2.231 GHz, and f_{IF} = 281 MHz, using standard register settings, maximum DGA gain, high linearity mode, unless otherwise noted. For IP2 and IP3 measurements, f_{RF1} = 1.949 GHz and f_{RF2} = 1.951 GHz, minimum DGA gain.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MIXER CHARACTERISTICS					
Voltage Conversion Gain		7		dB	
Input P1dB					
High Linearity Mode		12		dBm	
Low Power Mode		4		dBm	
Second-Order Input Intercept (IIP2)		55		dBm	0 dBm per tone, minimum DGA gain
Third-Order Input Intercept (IIP3)					0 dBm per tone, minimum DGA gain
High Linearity Mode		29		dBm	
Low Power Mode		17		dBm	
SSB NF					
RF = 1950 MHz		12		dB	
LO to RF Leakage		−30		dBm	
LO to IF Leakage		−40		dBm	
RF to IF Leakage		−50		dBc	Relative to IF output level
IF DGAs					
Voltage Gain		22		dB	
Gain Step		0.5		dB	
Gain Conformance Error		0.05		dB	Any two adjacent steps
Phase Conformance Error		0.5		Degrees	Any two adjacent steps
Output P1dB		19		dBm	
Output IP3 (OIP3)		40		dBm	
Bandwidth		520		MHz	
SSB NF		7		dB	
Second Harmonic Level		−65		dBc	At 2 V p-p
Third Harmonic Level		−65		dBc	At 2 V p-p

TIMING SPECIFICATIONS

MIX_AV_{DD} = MIX_BV_{DD} = DV_{DD} = LOV_{DD} = DGA_AV_{DD} = DGA_BV_{DD} = 3.3 V ± 5%; AGND = 0 V. 1.8 V and 3.3 V logic levels used. T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LE Setup Time	t_1	20			ns	
DATA to CLK Setup Time	t_2	10			ns	
DATA to CLK Hold Time	t_3	10			ns	
CLK High Duration	t_4	25			ns	
CLK Low Duration	t_5	25			ns	
CLK to LE Setup Time	t_6	10			ns	
LE Pulse Width	t_7	20			ns	
CLK Low to SDO Output Valid	t_8			20	ns	During readback

Timing Diagram

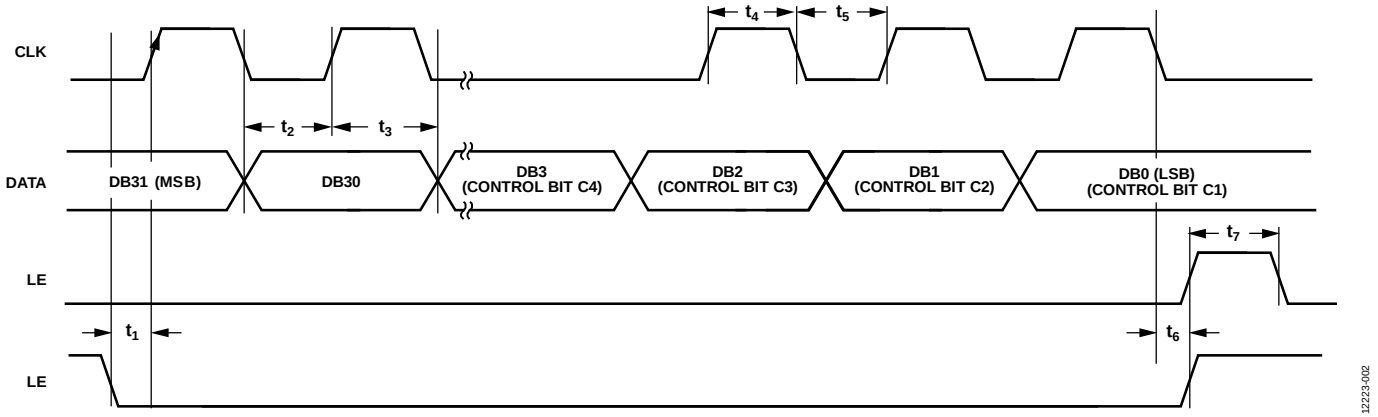

Figure 2. SPI Write Operation Timing Diagram

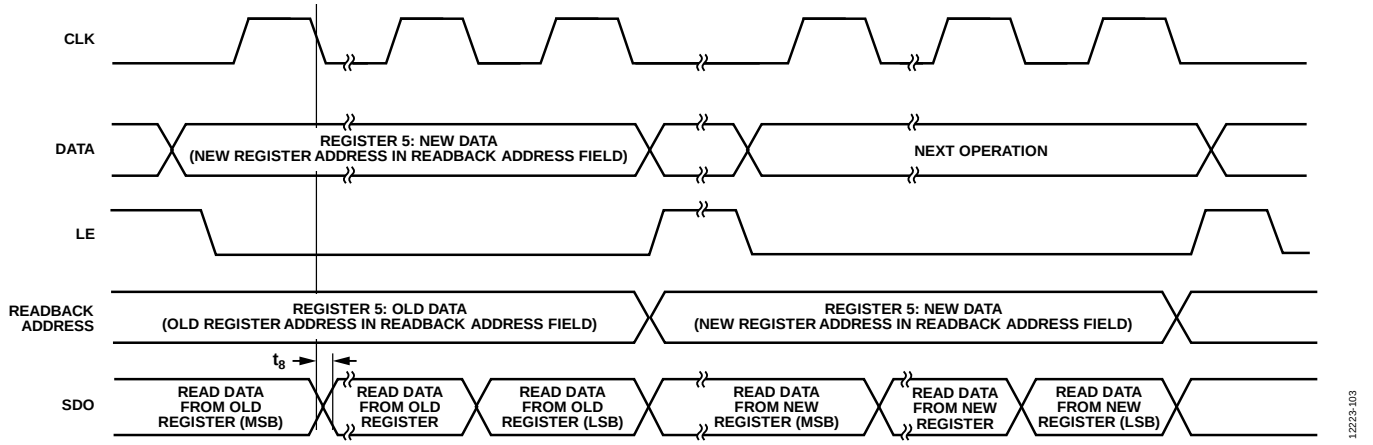

Figure 3. SPI Readback Operation Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
Supply Voltage Pins[1] to GND[2]	−0.3 V to +3.9 V
Supply Voltage Pins[1] to DV_{DD}	−0.3 V to +0.3 V
Digital Input Output (I/O) Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
RF Input Power	20 dBm
LO Input Power	10 dBm
ESD Ratings	
Human Body Model (HBM)	1.5 kV
Field Induced Charged Device Model (FICDM)	500 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Thermal Resistance (θ_{JA}), with Exposed Pad Soldered	27.26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] The supply voltage pins include MIX_AV_{DD}, DV_{DD}, MIX_BV_{DD}, DGA_BV_{DD}, LOV_{DD}, and DGA_AV_{DD}.
[2] GND = AGND = DGND = 0 V
[3] The digital I/O pins include $LATCH_A$, CH_AEN, CH_BEN, $LATCH_B$, B5 to B0, LE, CLK, DATA, SDO, and A0 to A5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The ADRF6658 is a high performance RF integrated circuit, and it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

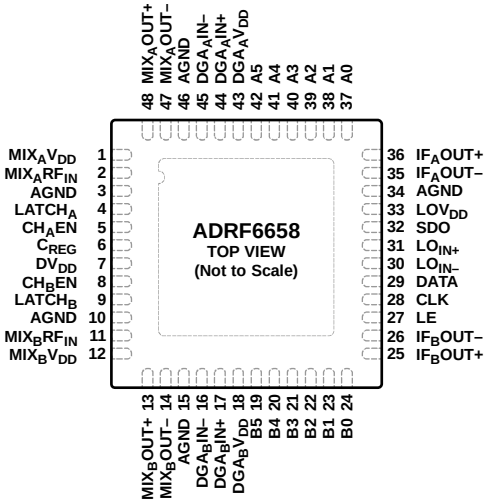

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MIX_AV_{DD}	Supply for Mixer A. The voltage level on this pin must be equal to that on DV_{DD}. Place decoupling capacitors to the ground plane as close as possible to this pin.
2	MIX_ARF_{IN}	RF Input for Mixer A. This pin has an input impedance of 50 Ω.
3	AGND	Analog Ground. This is a ground return path for MIX_AV_{DD} (Pin 1).
4	$LATCH_A$	Channel A Latch Buffer Control. This pin controls the latch buffer between the 6-bit parallel control port (Pin A0 to Pin A5) and the Channel A DGA.
5	CH_AEN	Channel A Enable. This pin provides external control of the power-down mode for Channel A.
6	C_{REG}	Internal Regulator Output. A capacitor of approximately 220 nF must be placed between this output and ground.
7	DV_{DD}	Supply Connection for Digital Circuits. The voltage on this pin ranges from 3.15 V to 3.45 V. Place decoupling capacitors to the ground plane as close as possible to this pin.
8	CH_BEN	Channel B Enable. This pin provides external control of the power-down mode for Channel B.
9	$LATCH_B$	Channel B Latch Buffer Control. This pin controls the latch buffer between the 6-bit parallel control port (Pin B0 to Pin B5) and the Channel B DGA.
10	AGND	Analog Ground. This is a ground return path for MIX_BV_{DD} (Pin 12).
11	MIX_BRF_{IN}	RF Input for Mixer B. This pin has an input impedance 50 Ω.
12	MIX_BV_{DD}	Supply for Mixer B. The voltage level on this pin must be equal to that on D_{VDD}. Place decoupling capacitors to the ground plane as close as possible to this pin.
13, 14	MIX_BOUT+, MIX_BOUT-	Differential Mixer B Outputs, 300 Ω Impedance. A pull-up inductor must be connected to each of these output pins. The values of the inductors depend on the IF frequency range.
15	AGND	Analog Ground. This is a ground return path for DGA_BV_{DD} (Pin 18).
16, 17	DGA_BIN-, DGA_BIN+	Differential DGA B Inputs, 300 Ω Impedance.
18	DGA_BV_{DD}	Supply for DGA B. The voltage level on this pin must be equal to that on DV_{DD}. Place decoupling capacitors to the analog ground plane as close as possible to this pin.
19, 20, 21, 22, 23, 24	B5, B4, B3, B2, B1, B0	6-Bit Parallel Control Ports for DGA B.
25, 26	IF_BOUT+, IF_BOUT-	Channel B Differential IF Outputs, 100 Ω Resistance from DGA B. Requires a pull-up inductor dependent on IF frequency.
27	LE	Latch Enable. When the LE input pin goes low, data is clocked into the 32-bit shift register on the CLK rising edge. Only the last 32 bits are retained. When the LE input pin goes high, the data stored in the shift register is loaded into one of the 16 registers, the relevant latch being selected by the four LSBs of the 32-bit word.

Pin No.	Mnemonic	Description
28	CLK	Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
29	DATA	Serial Data Input. The serial data input is loaded MSB first with the four LSBs control the destination for the data. This input is a high impedance CMOS input.
30	LO_{IN-}	Complimentary External Local Oscillator Input. In differential LO mode, this pin is one of the input pins of the differential input and must be ac-coupled. In single-ended LO mode, terminate this pin to ground with a capacitor.
31	LO_{IN+}	External Local Oscillator Input. In differential LO mode, this pin one of the input pins of the differential input. In single-ended LO mode, it is the input of the LO signal. AC couple this pin.
32	SDO	Serial Data Output. This output is used to read back the register content.
33	LOV_{DD}	Power Supply for the LO Path. The voltage level on this pin must be equal to that on DVDD. Place decoupling capacitors to the ground plane as close as possible to this pin.
34	AGND	Analog Ground. This is a ground return path for LOV_{DD} (Pin 33).
35, 36	IF_AOUT-, IF_AOUT+	Channel A Differential IF Outputs, 100 Ω Resistance from DGA A. Requires a pull-up inductor dependent on IF frequency.
37, 38, 39, 40, 41, 42	A0, A1, A2, A3, A4, A5	6-Bit Parallel Control Ports for DGA A.
43	DGA_AV_{DD}	Supply for DGA A. The voltage level on this pin must be equal to that on DV_{DD}. Place decoupling capacitors to the analog ground plane as close as possible to this pin.
44, 45	DGA_AIN+, DGA_AIN-	Differential DGA A Inputs, 300 Ω Impedance.
46	AGND	Analog Ground. This is a ground return path for DGA_AV_{DD} (Pin 43).
47, 48	MIX_AOUT-, MIX_AOUT+	Differential Mixer A Outputs, 300 Ω Impedance. A pull-up inductor must be connected to each of these output pins. The values of the inductors depend on the IF frequency range.
49	EP	Exposed Pad. Connect the exposed pad to ground through a low impedance path, using an array of vias from the pad to the PCB ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

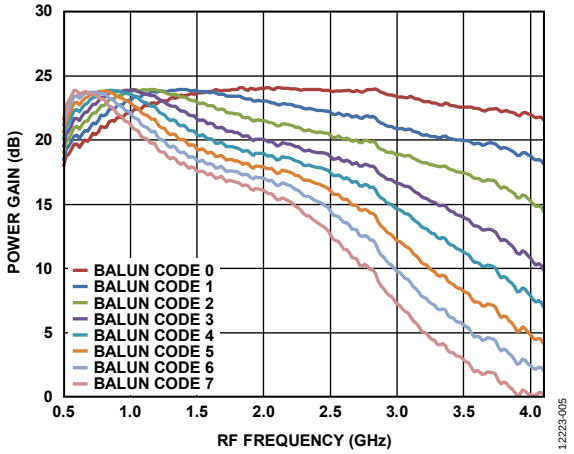

Figure 5. Power Gain vs. RF Frequency and Balun Codes

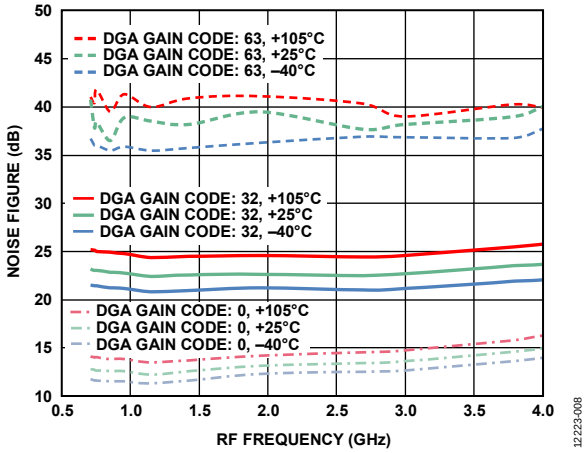

Figure 8. Noise Figure vs. RF Frequency and DGA Gain Codes

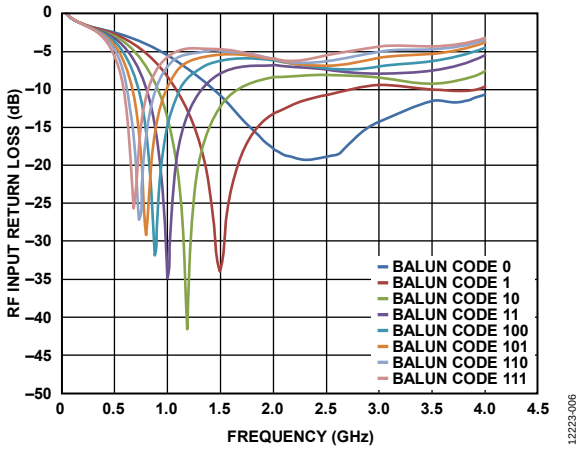

Figure 6. RF Input Return Loss vs. Frequency and Balun Codes

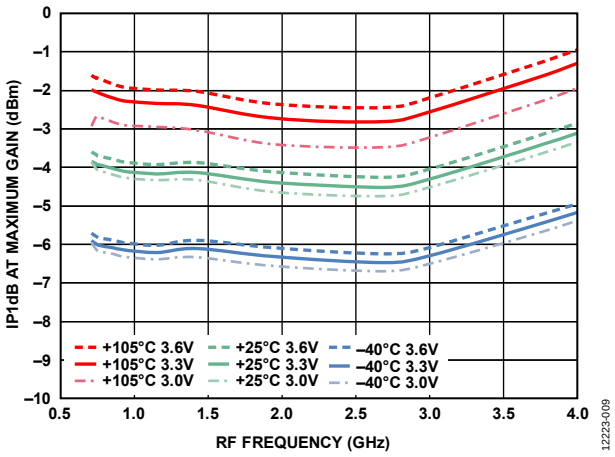

Figure 9. Input P1dB (IP1dB) vs. RF Frequency, DV_{DD} at Maximum Gain

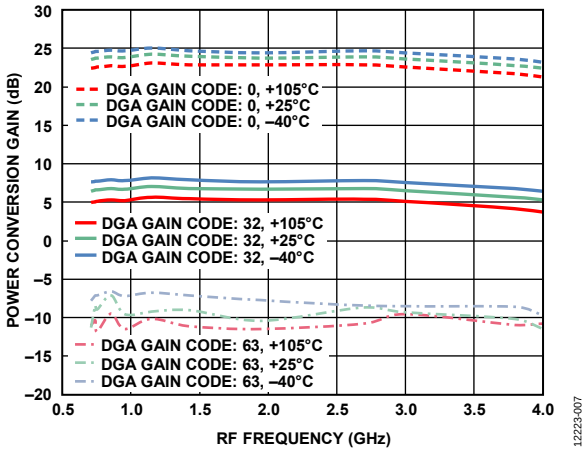

Figure 7. Power Conversion Gain vs. RF Frequency for DGA Gain Code = 0, 32, and 63

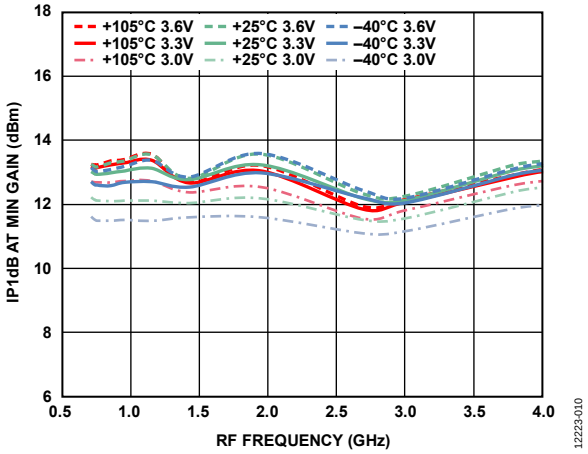

Figure 10. IP1dB vs. RF Frequency and DV_{DD} at Minimum Gain

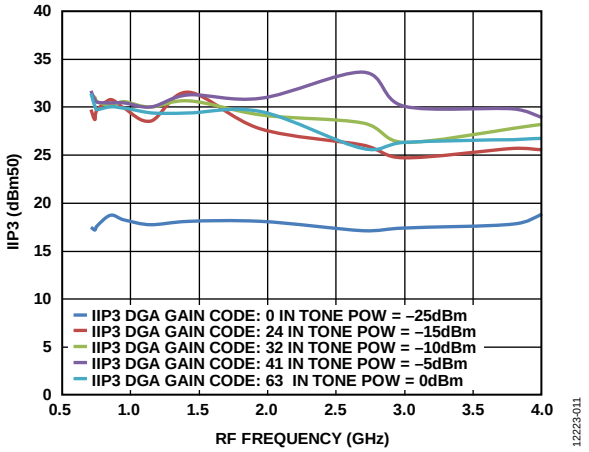

Figure 11. IIP3 vs. RF Frequency

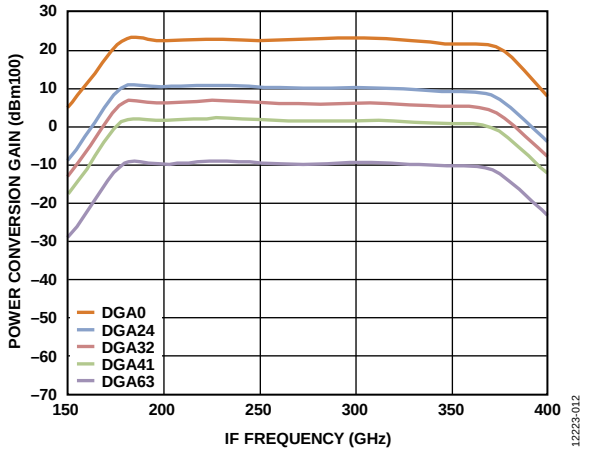

Figure 12. Power Conversion Gain vs. IF Frequency

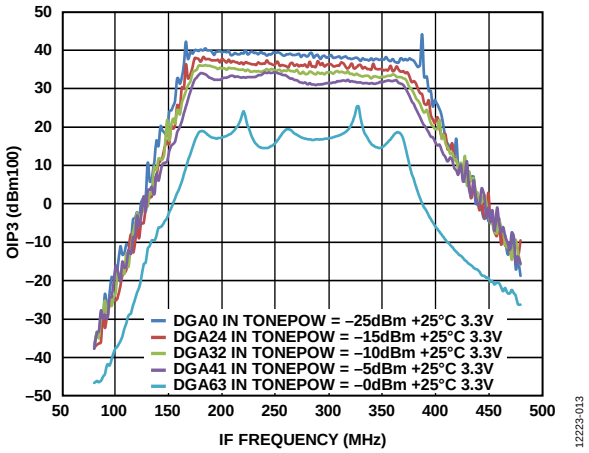

Figure 13. OIP3 vs. IF Frequency

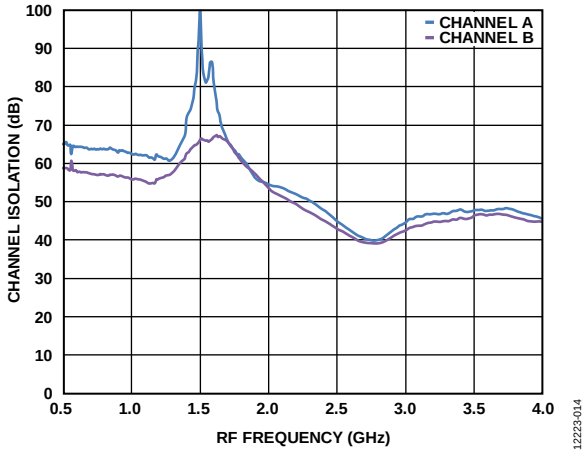

Figure 14. Channel Isolation

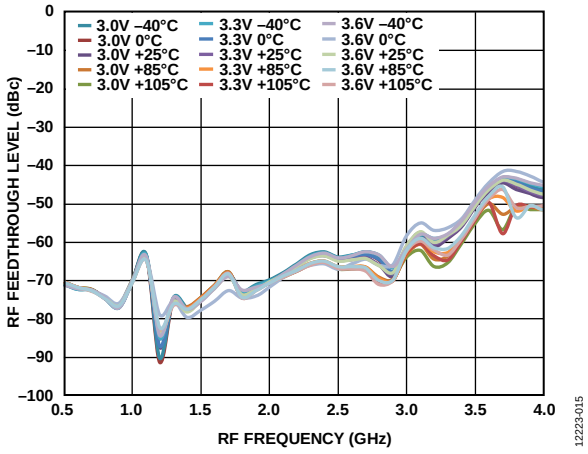

Figure 15. RF Feedthrough at Maximum Gain, Relative to IF Output Level

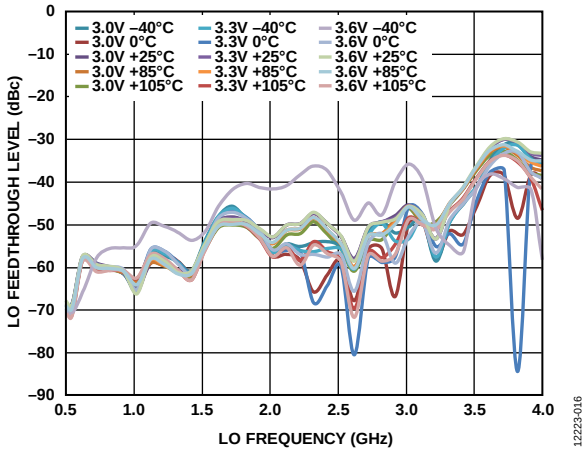

Figure 16. LO Feedthrough at Maximum Gain, Relative to IF Output Level

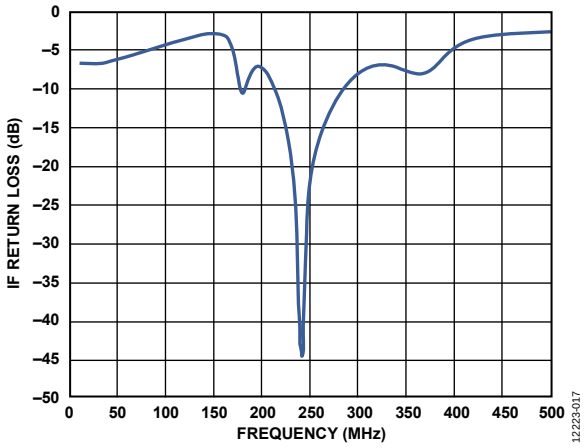

Figure 17. IF DGA Output Return Loss Measured Through Balun

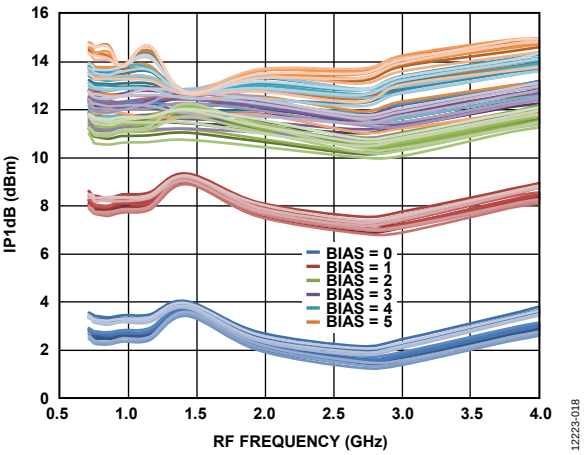

Figure 18. IP1dB vs. RF Frequency and V to I Bias

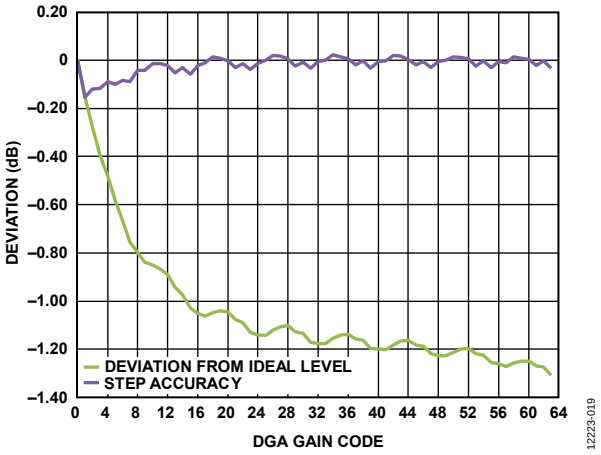

Figure 19. DGA Step Accuracy

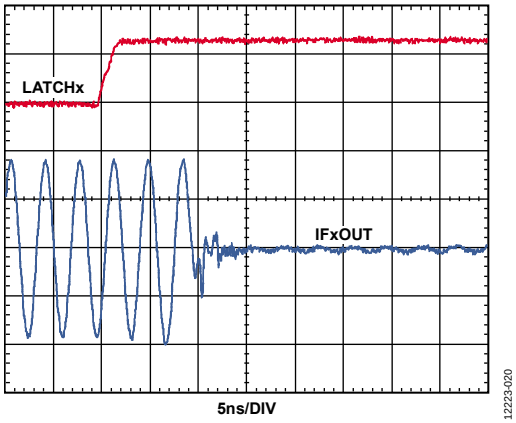

Figure 20. Gain Step Response, Maximum Gain to Minimum Gain

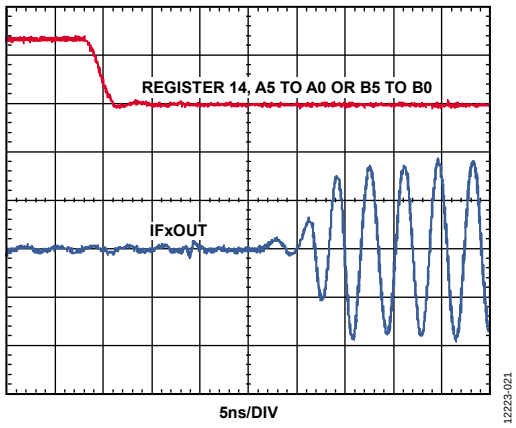

Figure 21. Gain Step Response, Minimum Gain to Maximum Gain

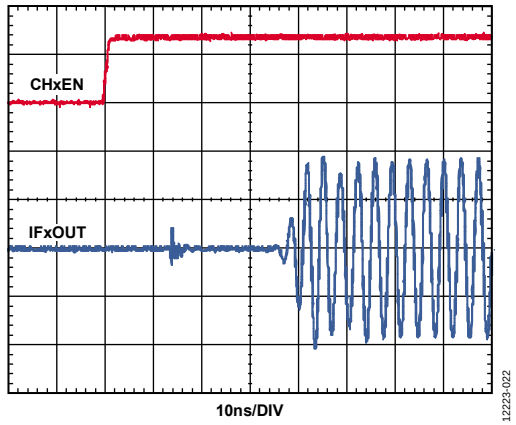

Figure 22. Channel Enable Response

THEORY OF OPERATION

DUAL MIXER CORES

The ADRF6658 provides two double balanced active mixers based on the Gilbert cell design. The RF inputs, LO inputs, and IF outputs of the mixers are all differential, providing maximum usable bandwidth at the input and output ports. The mixers are designed for a 50 Ω input impedance and a 300 Ω output impedance, with external RF chokes connected to the supply.

Mixer RF Inputs

At the RF input of each channel (MIX_ARF_{IN} and MIX_BRF_{IN}) of the ADRF6658, a tunable balun converts the single-ended input signal into differential form, to be fed into the mixer section. The tuning of the balun is controlled by the two sets of register bits: RF balun input cutoff (C_{IN}) in Register 13, Bits[DB12:DB10], and RF balun output cutoff (C_{OUT}) in Register 13, Bits[DB9:DB7].

Mixers Bias Circuit

A band gap reference circuit generates the reference currents used by mixers. The bias current for the LO circuit of the mixers can be programmed via the mixer LO I_{BIAS} bits in Register 13, Bits[DB26:DB25].

RF Voltage to Current (V to I) Converter

The differential RF input signal, created in the internal balun from the external, single-ended RF signal provided to the MIX_ARF_{IN} or MIX_BRF_{IN} pin, is applied to a V to I converter that converts the differential input voltage to output currents. The V to I converter provides a 50 Ω input impedance. The V to I section bias current can be adjusted up or down using the mixer V to I I_{BIAS} bits in Register 13, Bits[DB24:DB22]. Adjusting the current up improves IIP3 and P1dB input, but degrades the SSB NF. Adjusting the current down improves the SSB NF but degrades IIP3 and the input P1dB. The conversion gain remains nearly constant over a wide range of mixer V to I I_{BIAS} settings, allowing the device to be adjusted dynamically without affecting the conversion gain. A setting of 3 or 4 provides a good trade-off of IP3 and SSB NF.

Mixer Power-Down

It is possible to power down either mixer by programming the relevant bits. For Channel A, program the Mixer A enable bit (Bit DB5 in Register 13). For Channel B, program the Mixer B Enable bit (Bit DB4 in Register 13). The mixers can be powered down independently.

Mixer Output

The mixer load uses a pair of 150 Ω resistors connected to the positive supply. This provides a 300 Ω differential output resistance, which matches the input impedance of the internal IF DGA block. Pull the mixer outputs to the positive supply externally using a pair of RF chokes, or by using an output transformer with the center tap connected to the positive supply. The mixer outputs are dc-coupled, and they can operate up to approximately 500 MHz into a 300 Ω load.

DGA BASIC STRUCTURE

In each channel, the ADRF6658 has a built-in, variable gain DGA. Each amplifier consists of a digitally controlled, passive attenuator of a 300 Ω differential input impedance followed by a highly linear transconductance amplifier with feedback. The output impedance of the gain amplifier is 100 Ω, differentially. The input impedance of the DGA block matches the output impedance of the internal mixer.

The gain of each amplifier can be programmed independently, either via the DGA control bits in the serial control registers, or via an external, 6-bit parallel port. The choice of serial or parallel control is determined by the DGA control select bit, Bit DB22 in Register 7. Programming this bit to 0 allows the gain to be set by programming Register 14 (Bits[DB17:DB12] for Channel A, or Bits[DB11:DB6] for Channel B). When the DGA Control Select bit is set to 1, the gain is set by the binary value applied to the 6-bit, external parallel control interface (Pin A5 through Pin A0 for Channel A, or Pin B5 through Pin B0 for Channel B).

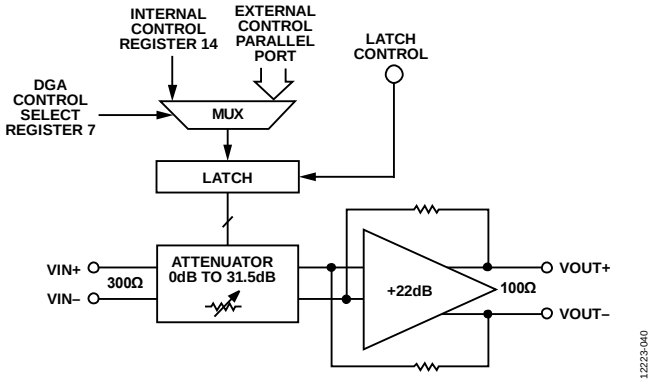

Figure 23. Simplified Schematic

Input System

The dc voltage level at the inputs of each amplifier is set to approximately 1.1 V by two independent internal voltage reference circuits. These reference circuits are not accessible and cannot be adjusted.

Power down each amplifier by setting Bit DB5 and Bit DB4.in Register 14. When powered down, the total current of each amplifier reduces to 10 µA (typical). The dc level at the inputs remains at approximately 1.6 V, regardless of the state of Bit DB5 and Bit DB4 in Register 14.

Output Amplifier

The gain of the output amplifier is set to 22 dB when driving a 100 Ω load. The input resistance of this amplifier is set to 300 Ω in matched condition, and its output resistance is set to 100 Ω. If the load resistance is different from 100 Ω, use the following equations to determine the resulting gain and input/output resistances:

$$A_V = 0.15 \times (3800)/R_L$$

$$R_{IN} = (3800 + R_L)/(1 + 0.15 \times R_L)$$

$$S21\ (Gain) = 2 \times R_{IN}/(R_{IN} + 300) \times A_V$$

$$R_{OUT} = (2000 + R_S)/(1 + 0.09 \times R_S)$$

where:
Av is the voltage gain.
R_L is the load resistance.
R_{IN} is the input resistance.
S21 is the insertion gain.
R_{OUT} is the output resistance.

Note that at the maximum attenuation setting, R_S, as seen by the output amplifier, is the output resistance of the attenuator, which is 300 Ω. However, at minimum attenuation, R_S is the source resistance connected to the DGA inputs of the device.

The dc current to the outputs of each amplifier is supplied through two external chokes. The inductance of the chokes and the resistance of the load, in parallel with the output resistance of the device, adds a low frequency pole to the response. The parasitic capacitance of the chokes adds to the output capacitance of the device. This total capacitance, in parallel with the load and output resistance, sets the high frequency pole of the device. Generally, the larger the inductance of the choke, the higher its parasitic capacitance. Therefore, this trade-off must be considered when the value and type of the choke are selected.

For an operation frequency of 45 MHz to 500 MHz when driving a 100 Ω load, 1.2 µH chokes with a self resonant frequency (SRF) of 375 MHz or higher are recommended (such as the 0805AF-122XJRB from Coilcraft). If higher value chokes are used, gain peaking may occur at the low frequency end of the pass band due to ac-coupling in the internal feedback path of the amplifier. The supply current of each amplifier takes about 80 mA through the two chokes combined in high linearity mode (Register 13, Bits[DB24:DB22] = 4). The current increases with temperature at approximately 2.5 mA per 10°C.

Gain Control

The gain of each amplifier can be adjusted using the parallel control interface or the SPI. The gain step size is 0.5 dB. Each amplifier has a maximum gain of +22 dB (Code 0) to −9.5 dB (Code 63). $LATCH_A$ or $LATCH_B$ must be at or transitioned to logic high after programming through the parallel or serial interface for the gain change to take effect.

The NF of each amplifier is approximately 4 dB at the maximum gain setting, relative to a 300 Ω source. This represents approximately 22.5 nV√Hz noise referred to the amplifier output. The NF increases as the gain is reduced, and this increase is equal to the reduction in gain. The linearity of the device measured at the output is first-order independent of the gain setting. From −4 dB to +22 dB gain, OIP3 is approximately 40 dBm into a 100 Ω load at 281 MHz (+1 dBm per tone). At gain settings below −4 dB, OIP3 drops to approximately 28 dBm.

SERIAL INPUT SHIFT REGISTERS

Data is clocked into the 32-bit shift register on each rising edge of CLK, MSB first. Data transfers from the shift register to one of sixteen latches on the rising edge of LE. The destination latch is determined by the state of the four control bits (C4, C3, C2, and C1) in the shift register. As shown in Figure 2, these are the four LSBs: DB3, DB2, DB1, and DB0. See Table 6 for the truth table for these bits. Figure 27 through Figure 42 describe the function of the control registers in the ADRF6658. The Register Maps section summarizes how to program the latches.

PROGRAM MODES

Table 6 and Figure 27 through Figure 42 show how to set up the program modes in the ADRF6658.

Table 6. Truth Table for Control Bits C4, C3, C2, and C1

Control Bits				
C4	**C3**	**C2**	**C1**	**Register**
0	0	0	0	Register 0 (R0)
0	0	0	1	Register 1 (R1)
0	0	1	0	Register 2 (R2)
0	0	1	1	Register 3 (R3)
0	1	0	0	Register 4 (R4)
0	1	0	1	Register 5 (R5)
0	1	1	0	Register 6 (R6)
0	1	1	1	Register 7 (R7)
1	0	0	0	Register 8 (R8)
1	0	0	1	Register 9 (R9)
1	0	1	0	Register 10 (R10)
1	0	1	1	Register 11 (R11)
1	1	0	0	Register 12 (R12)
1	1	0	1	Register 13 (R13)
1	1	1	0	Register 14 (R14)
1	1	1	1	Register 15 (R15)

REGISTER MAPS

REGISTER 0

RESERVED																									RESERVED	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED																											CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2

RESERVED																											CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED																											CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED																											CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(1)	C2(0)	C1(0)

REGISTER 5

READBACK ADDRES				RESERVED			SDO LEVEL	RESERVED																			CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RA4	RA3	RA2	RA1	0	0	0	SDL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(1)	C2(0)	C1(1)

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Figure 24. Register Summary (Register 0 Through Register 5)

REGISTER 6

RESERVED											DAISY-CHAIN EN	RESERVED				LOIN STANDBY	RESERVED				PU LO BIAS	RESERVED	PU LO IN	RESERVED				CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	1	0	0	0	0	0	DCE	0	0	1	0	LOS	0	0	1	0	PLB	0	PLI	0	0	0	0	C4(0)	C3(1)	C2(1)	C1(0)

REGISTER 7

RESERVED									DGA CONTROL SELECT	RESERVED																		CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	DCS	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	C4(0)	C3(1)	C2(1)	C1(1)

REGISTER 8

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(0)	C1(0)

REGISTER 9

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(0)	C1(1)

REGISTER 10

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(0)

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Figure 25. Register Summary (Register 6 Through Register 10)

REGISTER 11

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(1)

REGISTER 12

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(0)

REGISTER 13

RESERVED					MIXER LO IBIAS		MIXER V TO I IBIAS			MIXER V TO I RDAC				MIXER V TO I CDAC					RF BALUN INPUT CUT OFF			RF BALUN OUTPUT CUT OFF			RESERVED	MIXER A ENABLE	MIXER B ENABLE	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	MB5	MB4	MB3	MB2	MB1	MR4	MR3	MR2	MR1	MC5	MC4	MC3	MC2	MC1	IC3	IC2	IC1	OC3	OC2	OC1	0	MAE	MBE	C4(1)	C3(1)	C2(0)	C1(1)

REGISTER 14

RESERVED														DGA A GAIN						DGA B GAIN						DGA A ENABLE	DGA B ENABLE	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	0	0	1	0	0	0	AG6	AG5	AG4	AG3	AG2	AG1	BG6	BG5	BG4	BG3	BG2	BG1	DAE	DBE	C4(1)	C3(1)	C2(1)	C1(0)

REGISTER 15

RESERVED															DGA LOW POWER MODE	RESERVED	MIXER STANBDY	RESERVED										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	DLP	0	MSB	0	0	0	0	0	0	0	0	0	1	C4(1)	C3(1)	C2(1)	C1(1)

12223-043

Figure 26. Register Summary (Register 11 Through Register 15)

REGISTER 0 THROUGH REGISTER 4

Program Register 0 through Register 4 with the assigned values as shown in the register maps, Figure 27 through Figure 31.

RESERVED																									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	C4(0)	C3(0)	C2(0)	C1(0)

12223-144

Figure 27. Register 0 (R0), Hexadecimal Code = 0x00000010

RESERVED																									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(0)	C2(0)	C1(1)

12223-145

Figure 28. Register 1 (R1), Hexadecimal Code = 0x00000001

RESERVED																									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(0)	C2(1)	C1(0)

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Figure 29. Register 2 (R2), Hexadecimal Code = 0x00000002

RESERVED																									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(0)	C2(1)	C1(1)

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Figure 30. Register 3 (R3), Hexadecimal Code = 0x00000003

RESERVED																									CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(1)	C2(0)	C1(0)

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Figure 31. Register 4 (R4), Hexadecimal Code = 0x38000004

REGISTER 5

Control Bits

Program Register 5 by setting Bits[C4:C1] to 0101. Figure 32 shows the input data format for programming this register.

Readback Address

The readback address bits, Bits[DB31:DB28], determine which register content is read on the SDO output. Readback functionality is explained in the Readback section.

SDO Output Level

Bit DB24 changes the logic level of the SDO output. When programmed to 0, the SDO output is compatible with a 1.8 V logic. When set to 1, the SDO output uses 3.3 V as the high level.

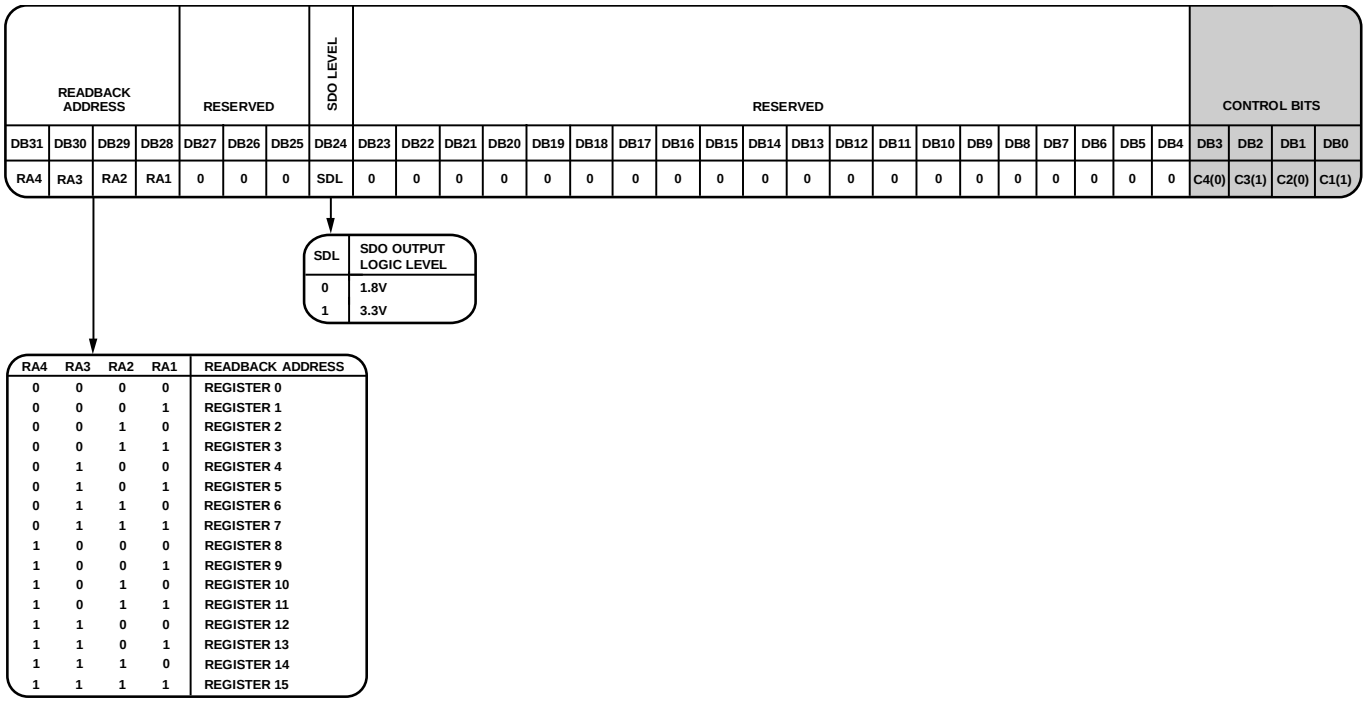


Figure 32. Register 5 (R5)

REGISTER 6

Control Bits

Program Register 6 by setting Bits[C4:C1] to 0110. Figure 33 shows the input data format for programming this register.

Daisy-Chain Enable

To enable daisy-chain mode for programming multiple devices, set Bit DB20 to 1. This feature is described in detail in the Daisy-Chain Mode section. Programming this bit to 0 disables this feature.

Local Oscillator Input Buffer Standby Mode

Bit DB15 controls the standby mode of the buffer on the LO input when both channels are disabled by pins CH_AEN and CH_BEN. In this case, if the LOIN standby bit is programmed to 0, the buffer on the LO input is in low power mode. When this bit is set to 1 while both channels are disabled, the buffer on the LO input works in normal mode, ensuring a shorter time of return to normal operation mode after any of the channels are enabled.

Bit DB8 controls the power up of the LO buffer. If DB8 is set to 0, the LO buffer is disabled.

Bit DB10 provides direct control of the LO buffer power modes. Set this bit to 1 for normal mode, and 0 for standby mode.

In normal operation mode, the LO input buffer typically consumes about 20 mA. In standby mode, this current is reduced to 6 mA.

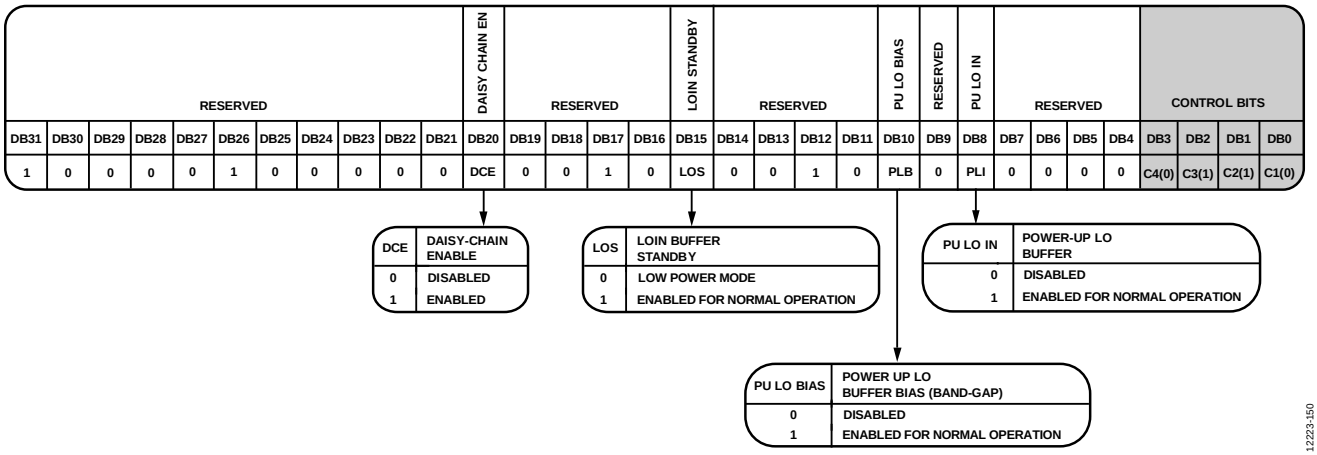


Figure 33. Register 6 (R6)

REGISTER 7

Control Bits

Program Register 7 by setting Bits[C4:C1] to 0111. Figure 34 shows the input data format for programming this register.

DGA Control Select

Bit DB22 selects the mode of control for the IF DGA. When this bit is programmed to 0, the gain of each DGA block is set by value of the relevant fields in Register 14: Bits[DB17:DB12] set the DGA A gain for Channel A, and Bits[DB11:DB6] set the DGA B gain for Channel B. When Bit DB22 in Register 7 is set to 1, the gain is controlled by the external parallel ports: Pin A5 through Pin A0 for Channel A, and Pin B5 through Pin B0 for Channel B.

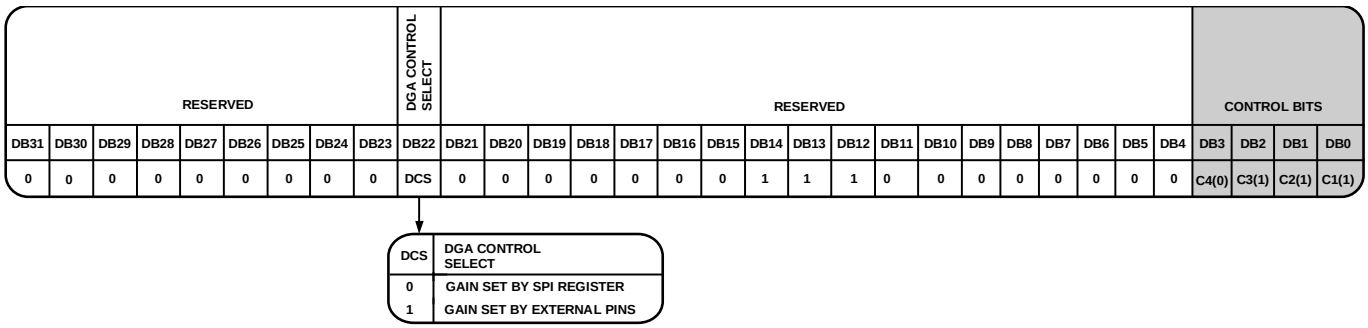


Figure 34. Register 7 (R7)

REGISTER 8 THROUGH REGISTER 12

Program Register 8 through Register 12 with the assigned values as shown in the register maps, Figure 35 through Figure 39.

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(0)	C1(0)

12223-047

Figure 35. Register 8 (R8), Hexadecimal Code = 0x00000008

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(0)	C1(1)

12223-048

Figure 36. Register 9 (R9), Hexadecimal Code = 0x00000009

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(0)

12223-049

Figure 37. Register 10 (R10), Hexadecimal Code = 0x0000000A

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(1)

12223-050

Figure 38. Register 11 (R11), Hexadecimal Code = 0x0000000B

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(0)

12223-051

Figure 39. Register 12 (R12), Hexadecimal Code = 0x0000000C

REGISTER 13

Control Bits

Program Register 13 by setting Bits[C4:C1] to 1101. This register controls the built in phase-locked loop (PLL) synthesizer. Figure 40 shows the input data format for programming this register.

Mixer LO Bias Current

Bits[DB26:DB25] set the value of the bias current of the mixer LO inputs.

Mixer V to I Converter Bias Current

Bits[DB24:DB22] set the value of the V to I converter bias current (I_{BIAS}) used on the mixer LO input.

Mixer V to I CDAC

Bits[DB17:DB13] set the value of CDAC bits that determines the capacitance component in the distortion correction circuit. These bits optimize the linearity correction in the mixer V to I converter as a function of RF frequency.

RF Balun Input Cutoff

Bits[DB12:DB10] select the input cutoff frequency of the balun on the RF mixer input.

RF Balun Output Cutoff

Bits[DB9:DB7] select the output cutoff frequency of the balun on the RF mixer input.

Mixer A Enabled

Bit DB5 powers up or switches off the mixer in Channel A. This option enables power saving if the mixer is not being used in the circuit.

Switching off Mixer A changes the supply current for this mixer from 80 mA to 5 mA.

Mixer B Enabled

Bit DB4 powers up or switches off the mixer in Channel B. This option enables power saving if the mixer is not being used in the circuit.

Switching off Mixer B changes the supply current for this mixer from 80 mA to 5 mA.

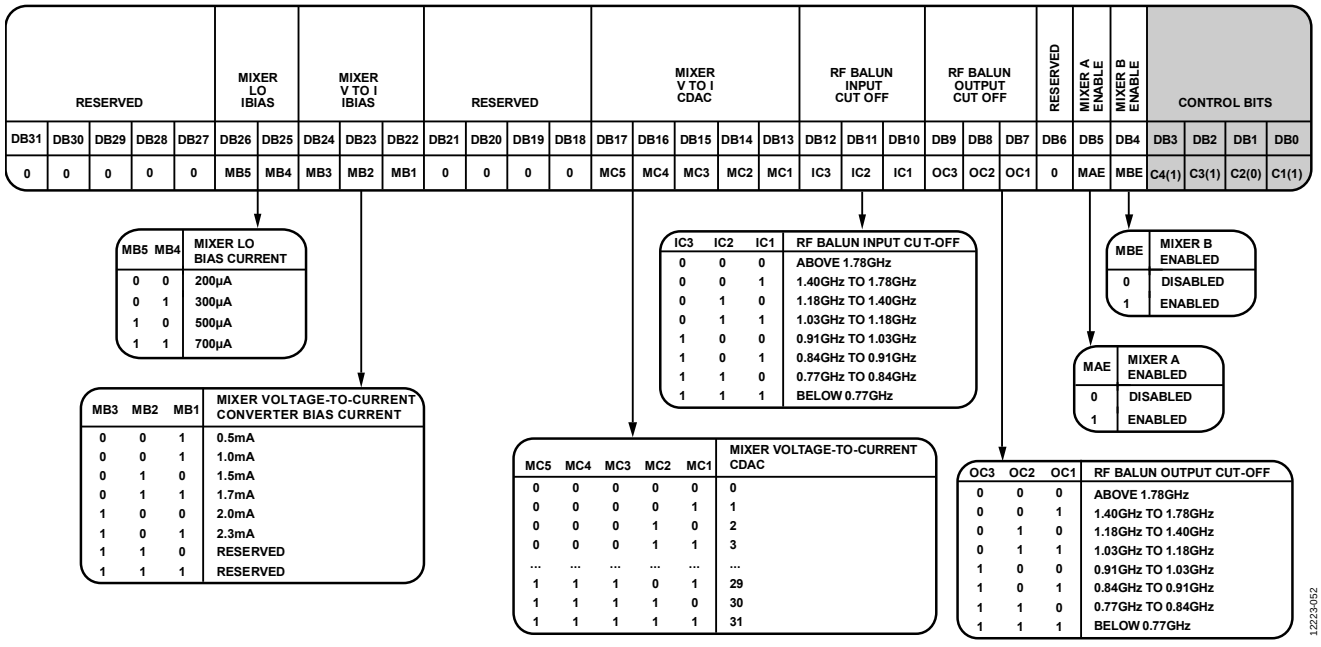


Figure 40. Register 13 (R13)

REGISTER 14

Control Bits

Program Register 14 by setting Bits[C4:C1] to 1110. This register controls the built in PLL synthesizer. Figure 41 shows the input data format for programming this register.

DGA Channel A Gain Control

Bits[DB17:DB12] set the gain in the DGA block in Channel A if the DGA control select bit (DCS, Register 7, Bit DB22) bit is 0. The gain is set by the value of the programmed attenuator in the DGA block in Channel A. The maximum value of the gain is +22 dB, and the minimum value is −9.5 dB. Figure 41 shows the corresponding values of the programmed gain and the binary word written to Bits[DB17:DB12]. $LATCH_A$ must be at logic low for the gain to change, and the new gain value is latched into the DGA when $LATCH_A$ goes high.

DGA Channel A Gain Control

Bits[DB11:DB6] set the gain in the DGA block in Channel B if the DCS bit (Register 7, Bit DB22) bit is 0. The gain is set by the value of the programmed attenuator in the DGA block in Channel B. The maximum value of the gain is +22 dB, and the minimum value is −9.5 dB. Figure 41 shows the corresponding values of the programmed gain and the binary word written to Bits[DB11:DB6].

DGA Channel A Enable

Bit DB5 powers up or powers down the DGA block in Channel A. To reduce the device power consumption, power down the DGA block in Channel A if not in use.

DGA Channel B Enable

Bit DB4 powers up or powers down the DGA block in Channel B. To reduce the device power consumption, power down the DGA block in Channel B if not in use.

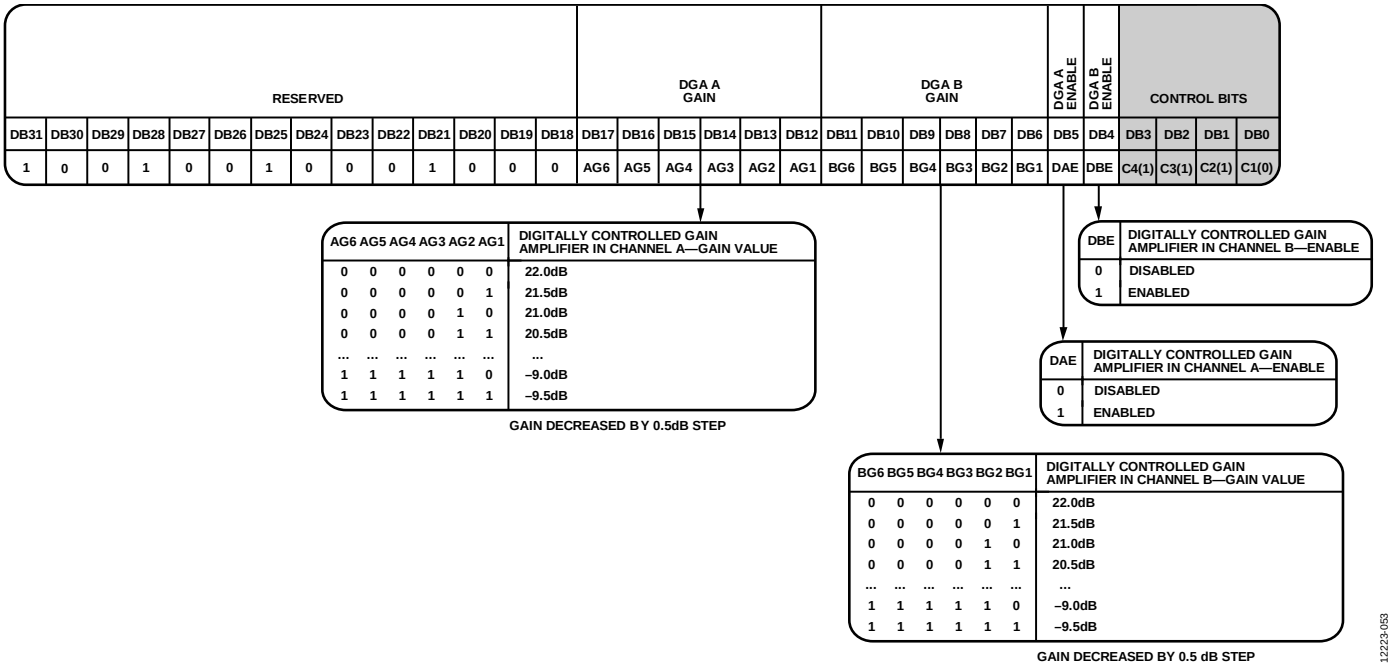


Figure 41. Register 14 (R14)

REGISTER 15

Control Bits

Program Register 15 by setting Bits[C4:C1] to 1111. This register controls the built in DGA block.

Figure 42 shows the input data format for programming this register.

DGAs—Low Power Mode

When set to 1, Bit DB16 enables the DGA low power mode. When programmed to 0, both DGA blocks work in normal mode.

In normal mode, the typical current used by each DGA block is approximately 140 mA. In low power mode, this current reduces to 23 mA.

Mixer Standby Mode

DB14 determines whether a mixer enters a low power mode or completely shuts off when the channel is disabled using Register 13, Bits DB4 and DB5. When DB14 is 0, the mixer is powered down. When DB14 is 1, the mixer stays in a low power mode. The band gap reference for the mixer bias circuit remains on in either case.

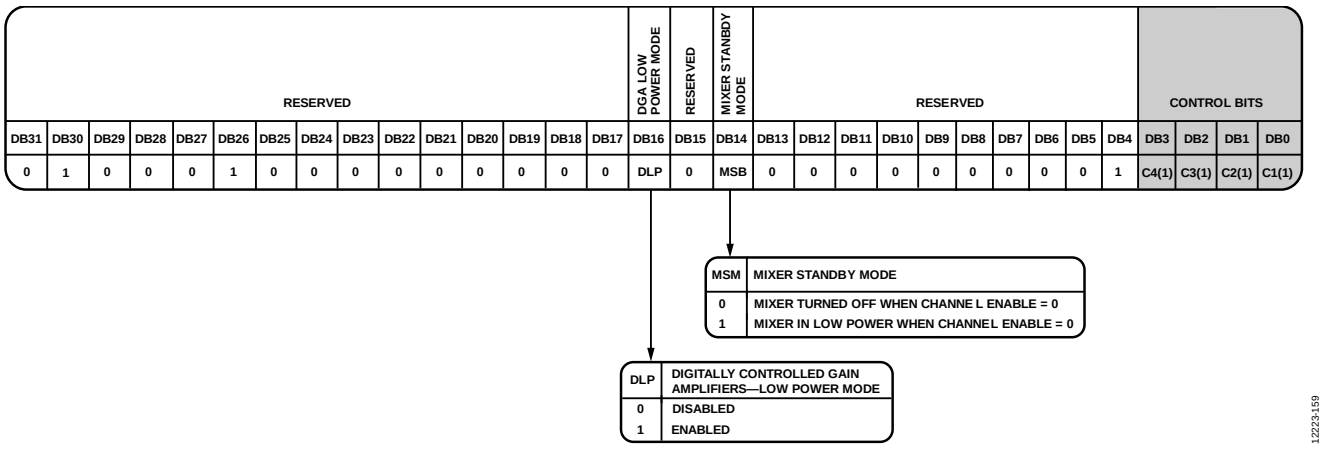


Figure 42. Register 15 (R15)

APPLICATIONS INFORMATION

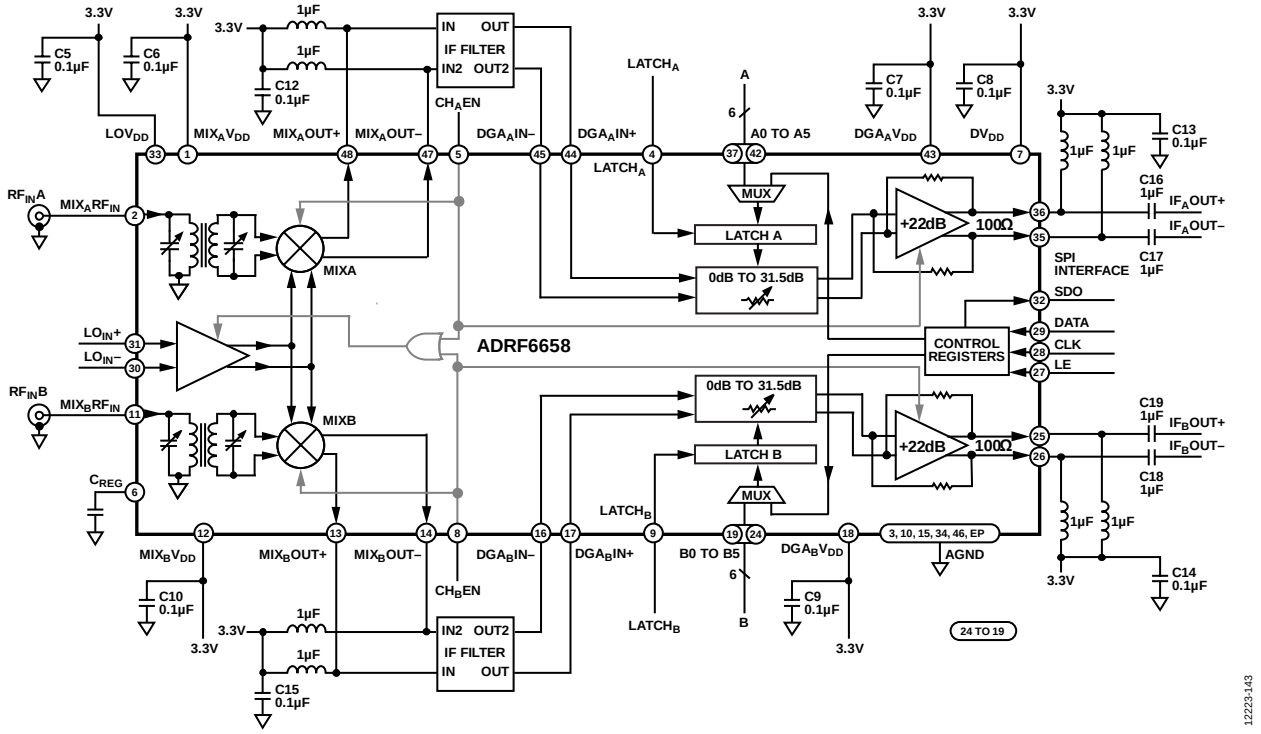


Figure 43. Basic Connections

BASIC CONNECTIONS

The basic connections for the ADRF6658 are shown in Figure 43.

INPUT TUNING

Conversion gain and input return loss can be optimized for an input frequency range

IIP3 Optimization

Input IP3 can be optimized by writing to the Mixer CDAC bits (Register 13, Bits[DB17:DB13]). Examples of optimum settings are listed in Table 7.

Table 7. IIP3 Optimization Settings

RF Frequency (MHz)	CDAC, Bits[DB17:DB13] (Decimal Value)	IIP3 for IF DGA at Minimum Gain (dBm)
750	26	36
900	25	32
1950	12	29
2700	10	25
3800	3	26

REGISTER INITIALIZATION SEQUENCE

At initial power-up, after applying correct voltages to the supply pins, the ADRF6658 registers load in the following sequence:

1. Register 15
2. Register 14
3. Register 13
4. Register 12
5. Register 11
6. Register 10
7. Register 9
8. Register 8
9. Register 7
10. Register 6
11. Register 5
12. Register 4
13. Register 3
14. Register 2
15. Register 1
16. Register 0

STANDARD REGISTER SETTINGS

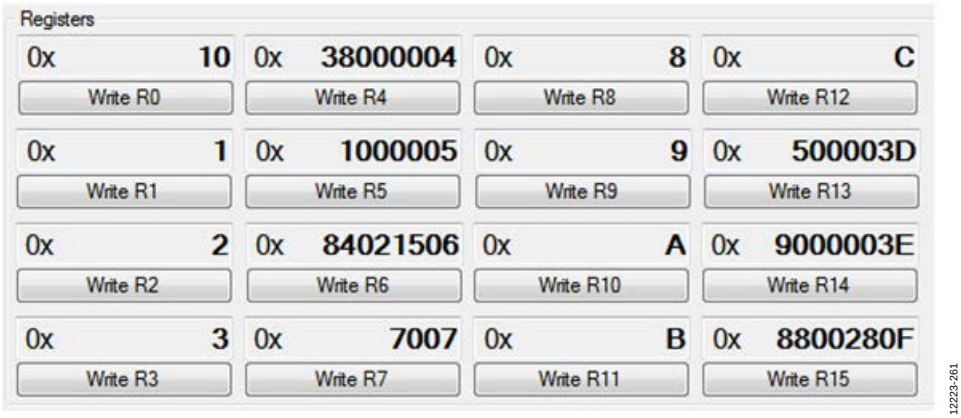


Figure 44. Register Settings for Standard Test Configuration

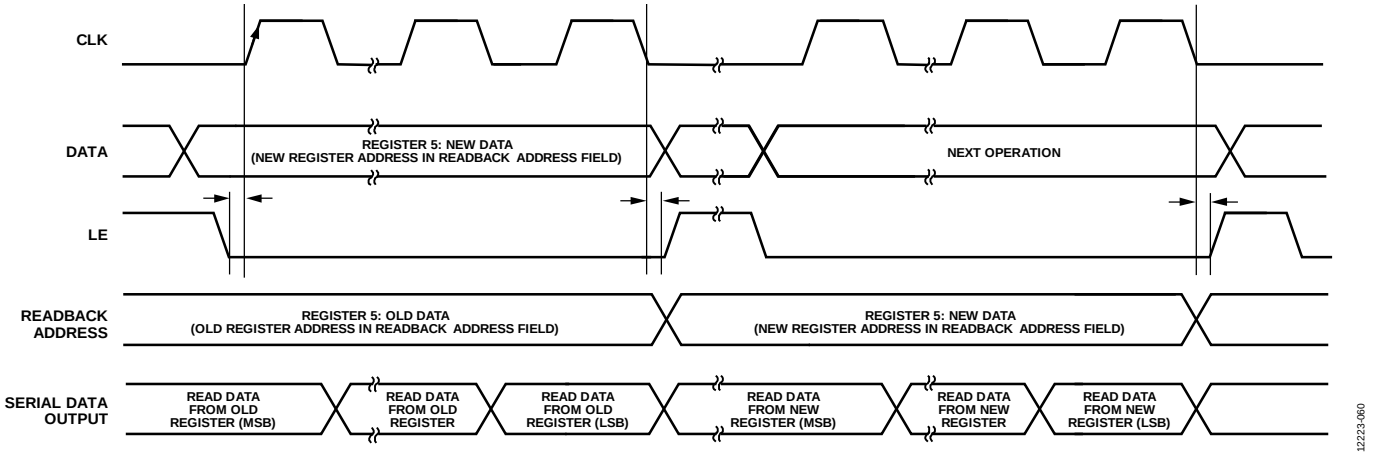


Figure 45. Timing Diagram for Readback Operation

READBACK

The address of the register that is read back is written to the readback address in Register 5, Bits[DB31:DB28].

After initialization of the device, the readback address stores a number from 0 to 15, depending on the value written to Bits[DB31:DB28] in Register 5. If the readback is performed after initialization but before a new value is written to the readback address field, the data read on the serial data output pin (the SDO pin) during the time of next write to the device (for example, during a new value write to Register 5) is the data stored in the register pointed to by the previous value of the readback address field. This is shown in Figure 45.

The data from new Register N, where N = 0 to 15, is available on the SDO output during the next write operation to the device after setting the correct register number by programming the readback address (Bits[DB31:DB28] in Register 5), as shown in Figure 45. To read the register values without changing the device settings, write a special no operation (NOP) command to the device. The format for this command is all zeros (0x00000000). Writing all zeros to Register 0 does not change any settings in this register due to the internal detection circuit, but allows the clock signal to be provided to the device so that readback can be performed.

DAISY-CHAIN MODE

In a system with one controller using the SPI for programming multiple devices, a dedicated signal for selecting a chip is used to address each device. In the ADRF6658, the function of chip select input is performed by the LE pin. As the number of devices increases, so does the number of lines used for device selection. Additionally, as both clock and data lines are routed from the controller outputs to the relevant inputs of each device, the layout become more complex. Using more outputs on the controlling device for the simple selection of different devices may become unacceptable due to the limited number of the controller outputs. In extreme situations, in a system with a numerous devices, additional controllers may be necessary to assure the correct addressing of each device.

To simplify the system, an alternative solution is the daisy-chain function, enabled by programming Bit DB20 in Register 6 of the ADRF6658. The daisy-chain function allows propagation of the signal through a string of slave devices, saving multiple outputs of the controller as well as simplifying the layout by removing multiple selection lines. The daisy chain also removes the necessity of connecting the data input of each slave device directly to the controller data output. To use the daisy chain, all slave devices must use the same SPI protocol.

Figure 46shows a traditional solution using multiple signals for selecting each device; Figure 47 shows a system using a daisy chain.

Writing to N independent devices in a traditional system demands programming each of the devices in sequence. As each write operation ends at a different time, so do the changes to the device settings. This may be a drawback for applications requiring synchronized changes to multiple devices. When using daisy-chain functionality, all slave devices must be programmed at the same time. To write to selected devices only, write an NOP command (0x00000000) to the devices requiring unchanged configuration. This command does not change any internal register settings of the device to which it is written.

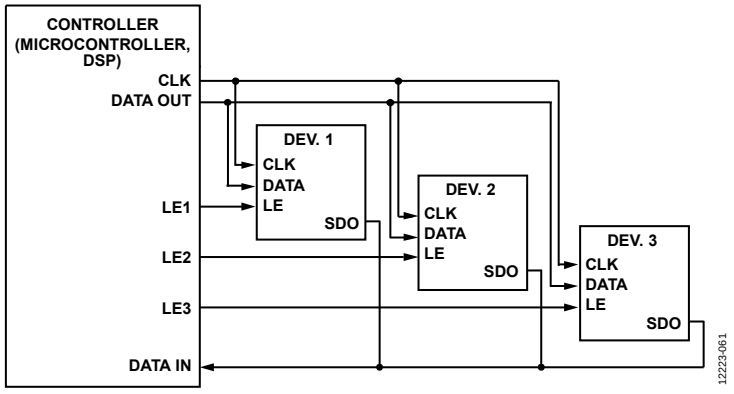


Figure 46. System with Traditional Multiple Chip Select

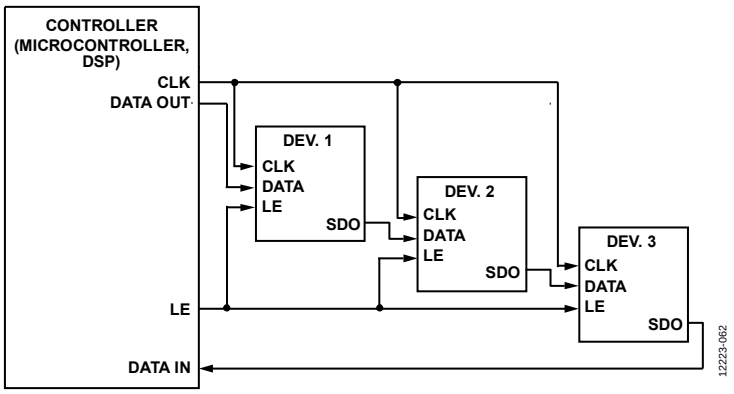


Figure 47. System with Daisy-Chain Functionality

Writing to a single, 32-bit register in each of the N devices with daisy chain functionality enabled is possible by writing N × 32 bits while the LE signal is kept low, then raising the LE signal. As new register settings are written to the device on the rising edge of the LE signal, the programmed register in multiple devices are updated at the same time. Figure 48 shows the timing diagram for writing to multiple devices.

During readback on a single device, the data available on the SDO output shows the content of the registers which addresses are currently stored in the readback address fields of the relevant devices. In daisy-chain mode, the data is written to or read from all the devices in sequence, as shown in Figure 49.

The data from the new Register M, where M = 0 to 15, is available on the SDO output during the next write operation to the device after setting the correct register number by programming the readback address (Bits[DB31:DB28] in Register 5), as shown in Figure 49. To avoid changing the register settings when readback is performed, an NOP command (0x00000000) can be used as the next operation.

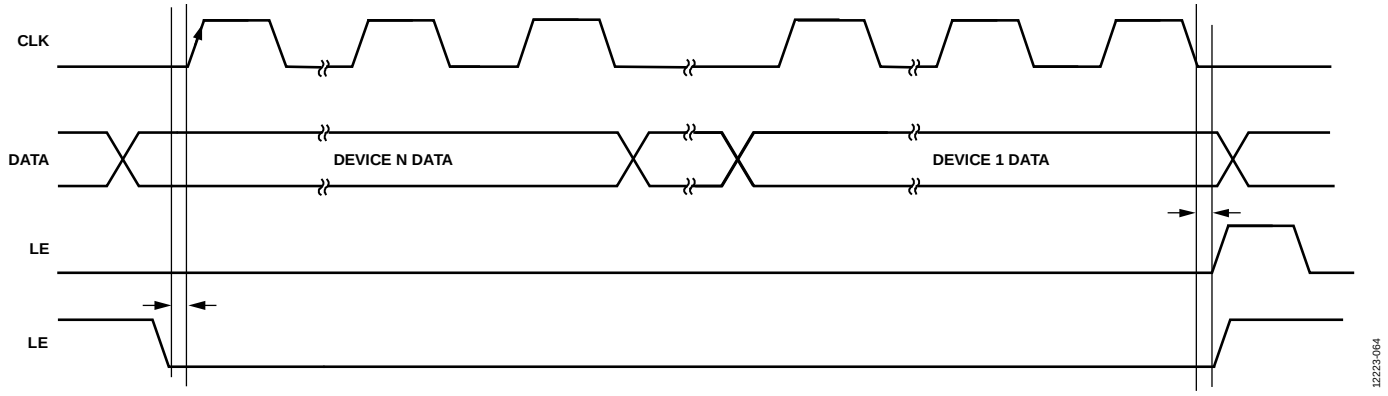


Figure 48. Timing Diagram for Writing to Multiple Devices Using Daisy-Chain Functionality for N Devices

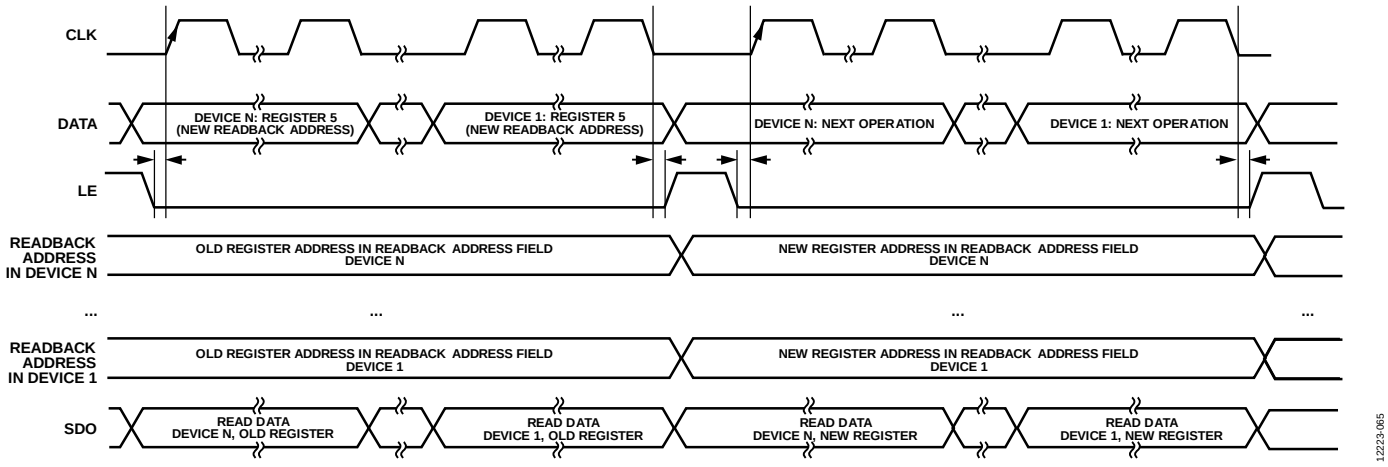


Figure 49. Timing Diagram for Readback from Multiple Devices Using Daisy-Chain Functionality for N Devices

IF FILTER

The IF filter used in the ADRF6658 evaluation is of a fifth order Butterworth design, shown in Figure 50, with a center frequency of 281 MHz and a bandwidth of 200 MHz.

The filter design is optimized to produce the best flatness and stop-band rejection at the presence of device parasitics, using standard Electronic Industries Association (EIA) E24 values, also known as standard 5% values.

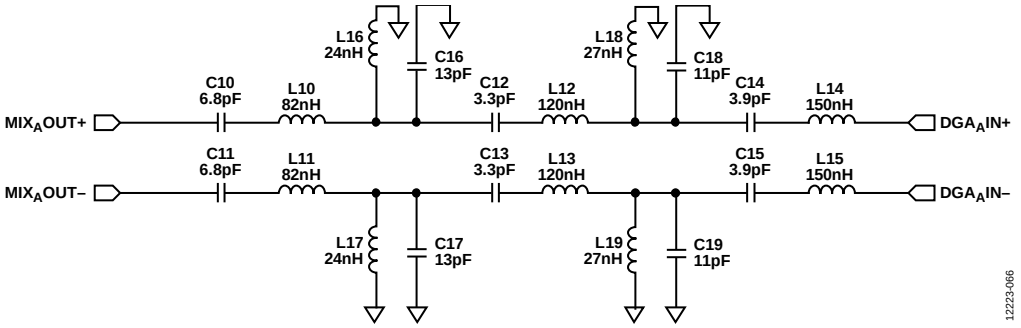
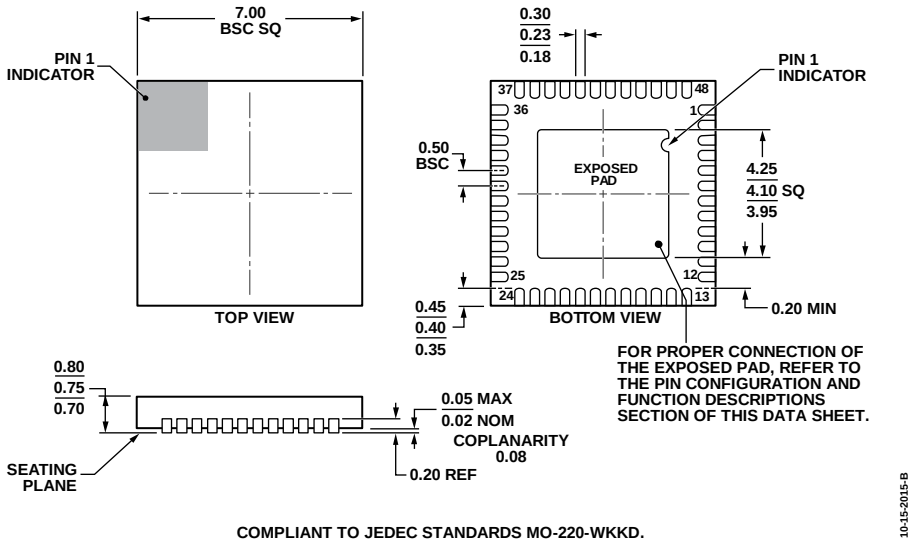


Figure 50. IF Filter

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD.

Figure 51. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6658BCPZ	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP], Tray	CP-48-5
ADRF6658BCPZ-RL7	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP], 7″ Tape and Reel	CP-48-5
EV-ADRF6658SD1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.