

PI6CU877 PI6CUA877

PLL Clock Driver for 1.8V DDR2 Memory

Features

- PLL clock distribution optimized for DDR2-667/533/400 SDRAM applications.
- Distributes one differential clock input pair to eleven differential clock output pairs.
- Differential Inputs (CLK, CLK) and (FBIN, FBIN)
- Input OE/OS: LVCMOS
- Differential Outputs $(Y[0:9], \overline{Y[0:9]} \text{ and } (FBOUT, \overline{FBOUT})$
- External feedback pins (FBIN, FBIN) are used to synchronize the outputs to the clock input.
- Operates at $AV_{DD} = 1.8V$ for core circuit and internal PLL, and $V_{DDQ} = 1.8V$ for differential output drivers
- Packaging (Pb-free & Green):
 52-ball VFBGA (NF)
- PI6CU877 for DDR2-533/400 applications
- PI6CUA877 for DDR2-667/533/400 applications

	0					
	1	2	3	4	5	6
А	Y1	Y ₀	Y ₀	¥5	Y5	Y ₆
В	$\overline{Y_1}$	GND	GND	GND	GND	$\overline{Y_6}$
С	$\overline{Y_2}$	GND	NB	NB	GND	<u>Y</u> 7
D	Y2	V _{DDQ}	V _{DDQ}	V _{DDQ}	OS	Y7
Е	СК	V _{DDQ}	NB	NB	V _{DDQ}	FB _{IN}
F	CK	V _{DDQ}	NB	NB	OE	FBIN
G	AGND	V _{DDQ}	V _{DDQ}	V _{DDQ}	V _{DDQ}	FB _{OUT}
Н	AV _{DD}	GND	NB	NB	GND	FB _{OUT}
J	Y3	GND	GND	GND	GND	Y ₈
k	¥3	$\overline{Y_4}$	Y ₄	Y9	¥9	Y ₈
						·

Pin Configuration

Description

PI6CU877 is a PLL clock driver family, consisting of PI6CU877, and PI6CUA877, developed for Registered DDR2 DIMM applications with 1.8V operation and differential clock input and output levels.

The device is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to eleven differential pairs of clock outputs which includes feedback clock (Y[0:9], $\overline{\text{Y[0:9]}}$; FBOUT, FBOUT).

The clock outputs are controlled by CLK/CLK, FBOUT, FBOUT, the LVCMOS inputs (OE, OS) and the Analog Power input (AV_{DD}). When OE is LOW the outputs except FBOUT, FBOUT, are disabled while the internal PLL continues to maintain its locked-in frequency. OS is a pin that must be tied to GND or V_{DD} . When OS is high, OE will function as described above. When OS is LOW, OE has no effect on Y7/Y7, they are free running. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When CLK/ $\overline{\text{CLK}}$ are logic low, the device will enter a low power mode. An input logic detection circuit will detect the logic low level and perform a low power state where all Y[0:9], $\overline{\text{Y}[0:9]}$; FBOUT, FBOUT, and PLL are OFF.

PI6CUx877 is a high-performance, low skew, and low jitter PLL clock driver, and it is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.



Block Diagram





Pinout Table

Pin Name	Characteristics	Description
AGND	Ground	Analog ground
AV _{DD}	1.8V nominal	Analog power
СК	Differential Input	Clock input with a (10k - 100k Ω) pulldown resistor
CK	Differential Input	Complementary clock input with a $(10k - 100k\Omega)$ pulldown resistor
FBIN	Differential Input	Feedback clock input
FBIN	Differential Input	Complementary feedback clock input
FB _{OUT}	Differential Output	Feedback clock output
FB _{OUT}	Differential Output	Complementary feedback clock output
OE	LVCMOS input	Output enable (async.)
OS	LVCMOS input	Output select (tied to GND or V _{DDQ})
GND	Ground	Ground
V _{DDQ}	1.8V nominal	Logic and output power
Y[0:9]	Differential Outputs	Clock outputs
<u>Y[0:9]</u>	Differential Outputs	Complementary clock outputs
NB		No Ball

Function Table

		Inputs			Outputs				PLL State
AV _{DD}	OE	OS	СК	CK	Y	Y	FBOUT	FBOUT	PLL State
GND	Н	Х	L	Н	L	Н	L	Н	Bypass/Off
GND	Н	Х	Н	L	Н	L	Н	L	Bypass/Off
GND	L	Н	L	Н	$L(Z)^{(1)}$	$L(Z)^{(1)}$	L	Н	Bypass/Off
GND	L	L	Н	L	L(Z) ⁽¹⁾ , Y7 active	$\frac{L(Z)^{(1)}}{Y7}$ active	Н	L	Bypass/Off
Nom. V _{DD}	L	Н	L	Н	$L(Z)^{(1)}$	$L(Z)^{(1)}$	L	Н	On
Nom. V _{DD}	L	L	Н	L	L(Z) ⁽¹⁾ , Y7 active	$\frac{L(Z)^{(1)}}{Y7}$ active	Н	L	On
Nom. V _{DD}	Н	Х	L	Н	L	Н	L	Н	On
Nom. V _{DD}	Н	Х	Н	L	Н	L	Н	L	On
Nom. V _{DD}	Х	Х	L	L	$L(Z)^{(1)}$	$L(Z)^{(1)}$	$L(Z)^{(1)}$	$L(Z)^{(1)}$	Off
Nom. V _{DD}	Х	Х	Н	Н	Reserved				

Notes:

1. L_(Z) means the outputs are disabled to a low state meeting the I_{ODL} limit on DC Specification



Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V _{DDQ} , A _{VDD}	I/O supply voltage range and analog /core supply voltage range	-0.5	2.5	
VI	V _I Input voltage range		V _{DDQ} +0.5	V
V _O	Output voltage range	-0.5	V _{DDQ} +0.5	
I _{IK}	Input clamp current	-50	50	
I _{OK}	Output clamp current	-50	50	
IO	Continuous output current, $V_O = 0$ to V_{DDQ}	-50	50	mA
I _{O(PWR)}	Continuous current through each VDDQ or GND	-100	100	
T _{STG}	Storage temperature	-65	150	°C

Note:

1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Specifications Recommended Operating Conditions

Symbol	Parameter		Min.	Nom.	Max.	Units
V _{DDQ}	Output Supply Voltage		1.7	1.8	1.9	
AV _{DD}	Supply voltage ⁽¹⁾			V _{DDQ}		
V _{IL}	Low-level input voltage ⁽²⁾ OE, OS, CK, \overline{CK}				0.35 x V _{DDQ}	V
V _{IH}	High-level input voltage OE , OS , CK , \overline{CK}		0.65 x V _{DDQ}			
I _{OH}	High-level output current, see Fig 2				-9	
I _{OL}	Low-level output current, see Fig. 2	Low-level output current, see Fig. 2			9	mA
V _{IX}	Input differential-pair crossing voltage		(V _{DDQ} /2) -0.15		(V _{DDQ} /2) -0.15	1117 1
V _{IN}	Input voltage level		-0.3		V _{DDQ} +0.3	
	Input differential voltage, See Fig 9	DC	0.3		V _{DDQ} +0.4	V
V _{ID}	(2)	AC	0.6		V _{DDQ} +0.4	
TA	Operating free air temperature		0		70	°C

Notes:

 The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and no timing parameters are guaranteed.

2. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} , see Figure 9 for definition. The CK and \overline{CK} , V_{IH} and V_{IL} limits are used to define the DC low and high levels for the logic detect state.

PI6CUx877	Operating Clock Frequency ^(1,2)		Application Cloc	Units	
Part Number	Min	Max	Min	Max	
PI6CU877	125	300	160	270	MHz
PI6CUA877	125	410	160	360	MHz

FCK Clock Frequency Specifications (AV_{DD}, V_{DDO} = 1.8 ±0.1V)

Notes:

1. The PLL is able to handle spread spectrum induced skew.

2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which it is not required to meet the other timing parameters. (Used for low-speed debug or production testing of DIMM modules).

3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.

Timing Requirements (Over recomended operating free-air temperature)

Symbol	Description	AV _{DD} , V _{DDQ} =	Units	
Symbol	Description	Min	Max	Units
t _{DC}	Input clock duty cycle	40	60	%
tL	t _L Stabilization time ⁽¹⁾		15	μs

 Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and CK go to a logic low state, enter the power-down mode and later return to active operation. CK and CK maybe left floating after they have been driven low for one complete clock cycle.



DC Specifications

Param- eter	Description	Test Condition	AV _{DD} , V _{DDQ}	Min.	Тур.	Max.	Units
V _{IK}	All Inputs	$I_{I} = -18mA$	1.7V			1.2	
V _{OH}	HIGH output voltage	$I_{OH} = -100 \mu A$	1.7 to 1.9V	V _{DDQ} -0.2			V
		$I_{OH} = -9mA$	1.7	1.1			
I _{ODL}	Output disabled low current	$OE = L, V_{ODL} = 100mV$		100			μA
V _{OD}	Output differential voltage, the magn between the true and complimentary more details		1.7V	0.6			V
T_	CK, CK	$V_I = V_{DDQ}$ or GND				±250	
II	OE, OS, FB_{IN} , $\overline{FB_{IN}}$	$V_I = V_{DDQ}$ or GND				±10	μA
I _{DDLD}	Static Supple current, $I_{DDQ} + I_{ADD}$	CK and $\overline{CK} = L$	1.9V			500	
I _{DD}	Dynamic supply current, I_{DDQ} + I_{ADD} , see note 6 for CPD calculation	CK and $\overline{CK} = 360 \text{MHz}$, all outputs are open (not connected to a PCB)				300	mA
	CK, CK	$V_I = V_{DDQ}$ or GND		2		3	
CI	FB _{IN} , FB _{IN}	$V_I = V_{DDQ}$ or GND	1.917	2		3	nE
	CK, CK	$V_I = V_{DDQ}$ or GND	1.8V			0.25	pF
$CI(\Delta)$	$FB_{IN}, \overline{FB_{IN}}$	$V_I = V_{DDQ}$ or GND				0.25	

Notes:

6. Total $I_{DD} = I_{DDQ} + I_{ADD} = F_{CKl} * C_{PD} * V_{DDQ}$, solving for $C_{PD} = (I_{DDQ} + I_{ADD})/(F_{CK} * V_{DDQ})$ where F_{CKl} is the input frequency, V_{DDQ} is the power supply and C_{PD} is the Power Dissipation Capacitance.

AC Specifications

Switching characteristics over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁵⁾

Damanatan	Description	Diagnam	AVDI	AV_{DD} , $V_{DDQ} = 1.8 \pm 0.1 V$			
Parameter	Description	Diagram	Min.	Nom.	Max.	Units	
ten	OE to and Y/Y	see Fig 11			8		
tdis	OE to and Y/Y	see Fig 11			8	ns	
tjit(cc+)	Cuele te suele iitter	and Fig.4	0		40		
tjit(cc-)	Cycle-to-cycle jitter	see Fig 4	0		-40]	
t(Ø)	Static phase offset ⁽¹¹⁾ see Fig 5 -50		50	1			
t(Ø)dyn	Dynamic phase offset	see Fig 10	-50		50		
tsk(o)	Output clock skew	see Fig 6			40	ps	
tjit(per)	Period jitter ⁽¹²⁾	see Fig 7	-40		40		
tiit(len en)	Half period jitter ⁽¹²⁾ 160 to 270 MHz	see Fig 8	-75		75		
tjit(hper)	Half period jitter ⁽¹²⁾ 271 to 360 MHz	see Fig 8	-50		50		
alr(i)	Input clock slew rate	see Fig 9	1	2.5	4		
slr(i)	Output enable (OE)	see Fig 9	0.5			V/ns	
slr(o)	Output clock slew rate ^(14, 16)	see Fig 1, 9	1.5	2.5	3		
V _{OX}	Outpu differential-pair cross voltage ⁽¹³⁾	see Fig 2	(V _{DDQ} /2) -0.1		(V _{DDQ} /2) +0.1	V	
The l	PLL on the PI6CUx877 is capable of meeting a with the f	Il the above test paramete		le supporting	SSC synthesire	rs	
SSC modulation frequency			30.00		33	kHz	
	SSC clock input frequency deviation		0.00		-0.50	%	
	PI6CUx877 PLL design should target th	e values below to	minimize the S	SCC induced	skew:		
	PLL Loop Bandwidth		2.0			MHz	

Notes:

- 11. Static Phase Offset does not include Jitter
- 12. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
- 13. VOX specified at the DRAM clock input or the test load.
- 14. To eliminate the impact of input slew rates on static phase offset, the input slew rates of Reference Clock Input CK, CK and Feedback Clock Input FBIN, FBIN are recommended to be nearly equal. The 2.5V/ns slew rates are shown as a recommended target. Compliance with these nominal values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
- 15. There are two terminations that are used with the above ac tests. The load/board in Figure 2 is used to measure the input and output differential-pair cross-voltage only. The load/board in Figure 3 is used to measure all other tests. For consistency, equal length cables should be used.
- 16. The Output slew rate is determined from IBIS model load shown in Figure 1. It is measured single-ended.









Figure 2. Output Load Test Circuit 1



Figure 3. Output Load Test Circuit 2





Figure 4. Cycle-to-Cycle Jitter



Figure 5. Static Phase Offset



Figure 6. Output Skew





Figure 7. Period Jitter (fo = average input frequency measured at CK/\overline{CK})



Figure 8. Half-Period Jitter



Figure 9. Input and Output Slew Rates





Figure 10. Dynamic Phase Offset



Figure 11. Time Delay Between Output Enable (OE) and Clock Output (\overline{Y}, Y)



Packaging Mechanical: 52-Ball VFBGA (NF)



Ordering Information^(1,2)

Ordering Code	Package Code	Package Description
PI6CU877NFE	NF	Pb-free & Green, 52-ball VFBGA
PI6CUA877NFE	NF	Pb-free & Green, 52-ball VFBGA

Notes:

1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/

2. E = Pb-free and Green