

October 2001 Revised October 2001

74ALVC162374 Low Voltage 16-Bit D-Type Flip-Flop with 3.6V Tolerant Inputs and Outputs and 26 Ω Series Resistors in Outputs

General Description

The ALVC162374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and output enable $(\overline{\text{OE}})$ are common to each byte and can be shorted together for full 16-bit operation

The ALVC162374 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceivers/transmitters.

The 74ALVC162374 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74ALVC162374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V-3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- \blacksquare 26 Ω series resistors in outputs
- t_{PD} (CLK to O_n)
 - 3.9 ns max for 3.0V to 3.6V $\rm V_{CC}$ 5.3 ns max for 2.3V to 2.7V $\rm V_{CC}$
 - 9.6 ns max for 1.65V to 1.95V $V_{\rm CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:

Human body model > 2000V

Machine model > 200V

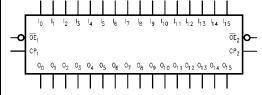
Note 1: To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Descriptions
74ALVC162374T	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Pin Descriptions

Pin Names	Description
OE _n	Output Enable Input (Active LOW)
CP _n	Clock Pulse Input
I ₀ -I ₁₅	Inputs
O ₀ -O ₁₅	Outputs

Connection Diagram

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015 - 23 26 - 115					
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	ŌĒ ₂ —	24		25	— CP ₂
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Truth Tables

	Inputs		Outputs
CP ₁	OE ₁	l ₀ –l ₇	00-07
\	L	Н	Н
~	L	L	L
L	L	Х	O ₀
Х	Н	Х	Z

	Inputs		Outputs
CP ₂	OE ₂	I ₈ -I ₁₅	O ₈ -O ₁₅
	L	Н	Н
~	L	L	L
L	L	Х	O ₀
Х	Н	Х	Z

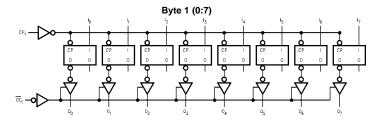
- H = HIGH Voltage Level
- = LOW Voltage Level = Immaterial (HIGH or LOW, inputs may not float)
- = High Impedance
- O_0 = Previous O_0 before HIGH-to-LOW of CP

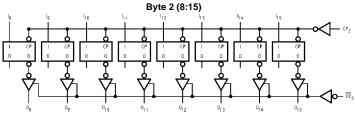
Functional Description

The 74ALVC162374 consists of sixteen edge-triggered flipflops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each clock has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-

flop will store the state of their individual I inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (\dot{CP}_n) transition. With the Output Enable (\overline{OE}_n) LOW, the contents of the flip-flops are available at the outputs. When \overline{OE}_n is HIGH, the outputs go to the high impedance state. Operations of the \overline{OE}_n input does not affect the state of the flip-flops.

Logic Diagram





Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

 $\begin{array}{lll} \mbox{Supply Voltage (V_{CC})} & -0.5 \mbox{V to } +4.6 \mbox{V} \\ \mbox{DC Input Voltage (V_I)} & -0.5 \mbox{V to } 4.6 \mbox{V} \end{array}$

Output Voltage (V_O) (Note 3) -0.5V to V_{CC} +0.5V

DC Input Diode Current (I_{IK})

 $V_1 < 0V$ -50 mA

DC Output Diode Current (I_{OK})

 $V_O < 0V$ DC Output Source/Sink Current

(I_{OH}/I_{OL})

DC V_{CC} or GND Current per

Supply Pin (I_{CC} or GND) ± 100 mA

Storage Temperature Range (T_{STG}) $-65^{\circ}C$ to $+150^{\circ}C$

Recommended Operating Conditions (Note 4)

Power Supply

-50 mA

±50 mA

Minimum Input Edge Rate (Δt/ΔV)

 $V_{IN} = 0.8V \text{ to } 2.0V, V_{CC} = 3.0V$ 10 ns/\

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V _{CC}		
			2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V _{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V _{CC}	
			2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V _{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	V _{CC} - 0.2		
		$I_{OH} = -2 \text{ mA}$	1.65	1.2		
		$I_{OH} = -4 \text{ mA}$	2.3	1.9		
		$I_{OH} = -6 \text{ mA}$	2.3	1.7		V
			3	2.4		
		$I_{OH} = -8 \text{ mA}$	2.7	2		
		$I_{OH} = -12 \text{ mA}$	3.0	2		
V _{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2	
		I _{OL} = 2 mA	1.65		0.45	
		I _{OL} = 4 mA	2.3		0.4	
		I _{OL} = 6 mA	2.3		0.55	V
			3		0.55	
		I _{OL} = 8 mA	2.7		0.6	
		I _{OL} = 12 mA	3		0.8	
I	Input Leakage Current	$0 \le V_1 \le 3.6V$	3.6		±5.0	μА
I _{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$	3.6		±10	μА
I _{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μΑ
ΔI_{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	μΑ

AC Electrical Characteristics

-		$T_A = -40$ °C to $+85$ °C, $R_L = 500\Omega$								
Symbol	Parameter	C _L = 50 pF			C _L = 30 pF				Units	
Зушьог	raiailletei	$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$\textrm{V}_{\textrm{CC}} = \textrm{2.5V} \pm \textrm{0.2V}$		$V_{CC}=1.8V\pm0.15V$		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	250		200		200		100		ns
t _{PHL} , t _{PL}	Propagation Delay Bus to Bus	1.3	3.9	1.5	5.3	1.0	4.8	1.5	9.6	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.3	4.4	1.5	5.9	1.0	5.4	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.3	4.5	1.5	4.9	1.0	4.4	1.5	7.9	ns
t _W	Pulse Width	1.5		1.5		1.5		4.0		ns
t _S	Setup Time	1.5		1.5		1.5		2.5		ns
t _H	Hold Time	1.0		1.0		1.0		1.0		ns

Capacitance

Symbol	Symbol Parameter		Conditions	T _A = -	Units	
Cymbol	Farameter		Conditions	V _{CC}	Typical	Units
C _{IN}	Input Capacitance		V _I = 0V or V _{CC}	3.3	6	pF
C _{OUT}	Output Capacitance		V _I = 0V or V _{CC}	3.3	7	pF
C _{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C _L = 50 pF	3.3	20	pF
				2.5	20	рі

AC Loading and Waveforms

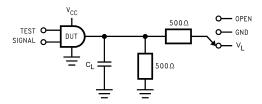


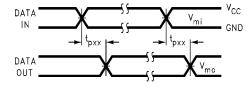
TABLE 1. Values for Figure 1

TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t_{PZL} , t_{PLZ}	V_{L}
t _{PZH} , t _{PHZ}	GND

FIGURE 1. AC Test Circuit

TABLE 2. Variable Matrix (Input Characteristics: f= 1MHz; $t_{r}=t_{f}=$ 2ns; $Z_{0}=50\Omega)$

Symbol		V	СС	
Cymbol	$3.3V \pm 0.3V$	2.7V	2.5V ± 0.2V	1.8V ± 0.15V
V _{mi}	1.5V	1.5V	V _{CC} /2	V _{CC} /2
V _{mo}	1.5V	1.5V	V _{CC} /2	V _{CC} /2
V _X	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V
V _Y	V _{OH} – 0.3V	V _{OH} – 0.3V	V _{OH} – 0.15V	V _{OH} – 0.15V
V _L	6V	6V	V _{CC} *2	V _{CC} *2



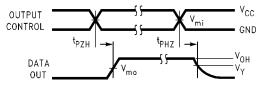


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

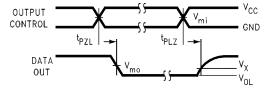


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

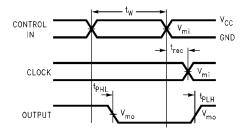


FIGURE 5. Propagation Delay, Pulse Width and $$t_{\mbox{\scriptsize REC}}$$ Waveforms

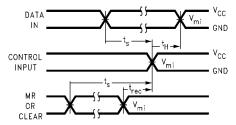
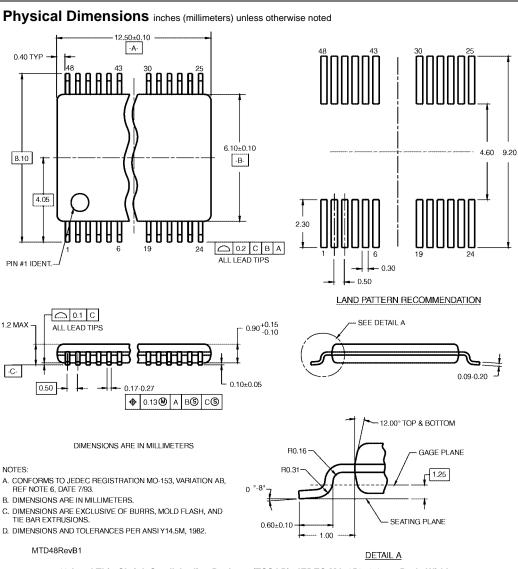


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic





48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Body Width Package Number MTD48

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