

Application Note: AS8506-AN02 – Passive Balancer

AS8506

AN02 – Passive Balancer



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Revision History

Revision	Date	Owner	Description
1.0	07.10.2013	gheh	Initial release



1 General Description

This document describes the AS8506 Passive Balancer Demo.

This kit demonstrates the AS8506 in conjunction with a host controller. Each board allows the balancing of up to 7 cells and multiple boards can be connected to support higher cell counts.

The hardware will support li-based cell packs as well as EDLCs.

Number of cells, target voltage as well as over and under voltage can be configured via a GUI

1.1 Kit Content

The kit consists of one double layer board with an 8 pin battery connector two stack connectors and a mini HDMI port to interface to the host controller and a mini-HDMI to micro-HDMI cable.



Figure 1: AS8506 Passive Board

2 Getting Started

To get started configure the device to your cell count and voltage specifications as described in chapter 4.

Also if you plan to connect multiple boards in a stack configure them as described in Section 4.3.

After having set up the hardware install the software that can be downloaded from: www.ams.com/DK-Passive-Board



Once finished with the installation connect the batteries to the boards, connect the master board via the provided HDMI cable to the USB Interface board and connect that to a PC via USB. Now fire up the PC GUI.

You should be all set to explore the possibilities of the chipset via the GUI interface. As described in Section 5

3 Hardware Description

The AS8506 Passive demo is powered via the battery connected via J1. Unconnected pins (in case lower cell counts then 7 are used) are shorted out by the bridging resistor and can be left unconnected.



Figure 2: PCB Top Side Diagram

Label	Name	Designator	Description	Info
A	BATT	J1	Battery Connector	Connects to 3 to 7 cells GND on the bottom
В	TOP_CONN	J2	Top Connection	To stack multiple boards
С	BOT_CONN	J3	Bottom Connection	To stack multiple boards
D	AMS_HDMI	J4	Master Connection	Connects to the USB Interface Board via provided cable
E	TEMP	J5	Temp Sensor	Can be connected to external temp sensor

Table 1: Connection Diagram





Figure 3: PCB Bottom Side Diagram

4 Configuration

4.1 Number of cells

Minimum number of cells to be balanced is 3 or as many to reach a battery voltage of at least 6V (cell chemistry / technology dependent). A maximum of 7 cells can be balanced by this board!

Cell-Nr	Remove
3	none
4	R4
5	R4, R3
6	R4, R3, R2
7	R4, R3, R2, R1

Remove zero ohm resistors according to table:

Table 2: Cell Adjust

4.2 **Configuration of VREF**

There are two options to set the balancing target voltage:

- 1. Defined by DAC via the GUI configuration interface
- 2. Defined by external voltage divider (has to be activated in the GUI)

In case the second option is chosen or if you want to switch between the options the divider R13, R14 needs to be selected according to number of cells according to the following table:



Cell-Nr	R14	R13
3	100K	200K
4	100K	300K
5	30K	120K
6	150K	750K
7	20K	120K

Table 3: VREF relative adjust

4.3 Configuration of master/slave

If you want to chain multiple devices you have to configure the chained devices into slave mode and unsolder the stack termination registers from all but the topmost board

Multiple devices can be connected via J2 and J3 which just plug together.

The lowest board always has to be the master. Meaning this board has to be configured as master (which is the factory setting) and this board is the one to connect to the USB Interface box.

To configure a board for slave mode you have to move the 0Ω Resistor R10 to R9.

Then you have to unsolder R5, R7 and R8 termination resistors from all but the topmost board.



Board 1 Stats Cel 1 3726ev/ 0 V UV 2 C REF Cel 2 3723ev/ 0 V UV 2 C REF Cel 3 3724ev/ 0 V UV 2 C REF Cel 4 3723ev/ 0 V UV 2 C REF Cel 4 3724ev/ 0 V UV 2 C REF Cel 5 3724ev/ 0 V UV 2 C REF Cel 6 3727ev/ 0 V UV 2 C REF Cel 6 3727ev/ 0 V UV 2 C REF Cel 7 3724ev/ 0 V UV 2 C REF Cel 7 3724ev/ 0 V UV 2 C REF Cel 6 3727ev/ 0 V UV 2 C REF Cel 7 3724ev/ 0 V UV 2 C REF VW 1 Prequency 100 Khz PKH PKH Prequency 100 Khz VW 1 Prequency 100 Khz PKH PKH Prequency 100 Khz PKH VW 1 VY 2 C REF Statt adress alocatin fall	ile <u>V</u> iew <u>S</u> ettings <u>H</u> el	p			
ControtTab GraphTab Board 1 Status Cell 1 3736mV OV UV 2C REF Cell 2 3733mV OV UV 2C REF Cell 3 3734mV OV UV 2C REF Cell 4 3734mV OV UV 2C REF Cell 2 3734mV OV UV 2C REF Cell 2 Cell 2 Over VUV 2C REF Cell 3 3734mV OV UV OV UV ZC REF Cell 5 3724mV OV UV ZC Cell 6 3735mV OV UV ZC REF VMI Frequency 100 KHz PMI	Register Map Readout Registers	Balance			am
Board 1 Chip D: 52768 Passive Ceil 1 3738mV OV UV 2C REF Ceil 2 3733mV OV UV 2C REF Ceil 3 3734mV OV UV 2C REF Ceil 4 3734mV OV UV 2C REF Ceil 5 3734mV OV UV 2C REF Ceil 4 3734mV OV UV 2C REF Ceil 5 3734mV OV UV 2C REF Ceil 6 3732mV OV UV 2C REF Ceil 7 3732mV OV UV 2C REF Temp 1 2LSB Ambient ML ML ML	ComfortTab GraphTab				
Board 1 Chip D: 52788 ♥ Passive Cell 1 3785mV OV UV 2 Cell 5 found: 14 Board 5 found: 2 3785mV OV UV 2 minimized for the second for	Boards		Status		
Cell 1 3780mV OV UV ZC REF Cell 2 3733mV OV UV ZC REF Cell 3 3734mV OV UV ZC REF Cell 4 3734mV OV UV ZC REF Cell 5 3734mV OV UV ZC REF Cell 4 3734mV OV UV ZC REF Cell 5 3734mV OV UV ZC REF Cell 4 3734mV OV UV ZC REF Cell 5 3734mV OV UV ZC REF Cell 6 3737mV OV UV ZC REF Cell 6 3737mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Temp 1 2 LSB Ambient: ML ML ML Temp 2 0 LSB Internat WL ML ML	Board 1		Chip ID:	52768	✓ Passive
Cell 1 3786mV OV UV 2C REF Cell 2 3733mV OV UV 2C REF Cell 3 3734mV OV UV 2C REF Cell 4 3734mV OV UV 2C REF Cell 5 3734mV OV UV 2C REF Cell 6 3737mV OV UV 2C REF Cell 6 3737mV OV UV 2C REF Cell 6 3737mV OV UV 2C REF Cell 7 3732mV OV UV 2C REF Cell 7 3732mV OV UV 2C REF Temp 1 2 LS8 Ambient: WL ML Temp 2 0 LS8 Internat WL ML	board I		Cells found:	14	
Cel 2 3733mV OV UV ZC REF Cel 3 3734mV OV UV ZC REF Cel 4 3734mV OV UV ZC REF Cel 4 3734mV OV UV ZC REF Cel 4 3734mV OV UV ZC REF Cel 5 3734mV OV UV ZC REF Cel 6 3737mV OV UV ZC REF Cel 7 3732mV OV UV ZC REF Cel 7 3732mV OV UV ZC REF Cel 7 3732mV OV UV ZC REF Temp 1 2 LSB Internal WL ML <	Cell 1 378	6mV OV UV ZC V REF	Boards found:	2	
Cell 2 3733mV OV UV ZC REF Cell 3 3734mV OV UV ZC REF Cell 4 3734mV OV UV ZC REF Cell 4 3734mV OV UV ZC REF Cell 5 3734mV OV UV ZC REF Cell 6 3737mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Temp 1 2 LSB Ambient: WL ML Temp 2 0 LSB Internat: WL ML			Status	Comm	unication Status
Cell 3 3734mV OV UV ZC REF Cell 4 3734mV OV UV ZC REF Cell 4 3734mV OV UV ZC REF Cell 5 3734mV OV UV ZC REF Cell 6 3737mV OV UV ZC REF Cell 6 3737mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Temp 1 2 LSB Ambient: WL ML Upper Threshold 4,000V Internal Temp 2 0 LSB Internat: WL ML Internat: Internat: <td< td=""><td>Cell 2 373</td><td>3mV OV UV ZC REF</td><td>Balance Done Cell Voltage or Temp n</td><td>ot OK</td><td>dress Allocation Fail PI3 read fail</td></td<>	Cell 2 373	3mV OV UV ZC REF	Balance Done Cell Voltage or Temp n	ot OK	dress Allocation Fail PI3 read fail
Cell 4 3734mV OV UV ZC REF Cell 5 3734mV OV UV ZC REF Cell 6 3737mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Temp 1 2 LSB Ambient: WL ML Temp 2 0 LSB internati WL ML	Cell 3 373	4mV OV UV ZC REF	Ver Voltage		PI3 write fail PI3 Broadcast fail RC Error M->S
Cell 5 3734mV OV UV ZC REF Cell 6 3737mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Cell 7 3732mV OV UV ZC REF Temp 1 2 LSB Ambient: WL ML Temp 2 0 LSB Internat: WL ML	Cell 4 373	4mV OV UV ZC REF	Cell Zero Cross Over Temperature		RC Error S->M tart adress allocation fail
Cell 6 3737mV OV UV ZC REF PWM Frequency 100 KHz PWM Duty Cycle 25% Comparator Cycles 5 clock cycles Cell 7 3732mV OV UV ZC REF Temp 1 2 LSB Ambient: WL ML Temp 2 0 LSB Internal	Cell 5 373	4mV OV UV ZC REF	Settings		
Cell 7 3732mV OV UV ZC REF Temp 1 2 LSB Ambient: WL ML Temp 2 0 LSB Internat WL ML	Cell 6 373	7mV 0V UV ZC REF	PWM Frequency PWM Duty Cycle	100 KHz 25%	
Temp 1 2 LSB Ambient: WL ML Upper Threshhold 4,000V Internal Internal Temp 2 0 LSB Internat: WL ML International	Cell 7 373	2mV 0V UV ZC REF	Comparator Cycles External resistor divider	5 clock cycles	
Temp 2 0 LSB Internat WL ML	Temp 1 2 LSB	Ambient: WL ML	Upper Threshhold 4,00 Lower Threshhold 3.00	0V	internal
Reference 3,740V internal	Temp 2 0 LSB	Internal: WL ML	Reference 3,74	10V	internal

5 Software Description

Figure 4: AS8506 GUI

Once started the PC GUI will automatically detect the AS8506 Boards connected to the USB Interface and enumerate those. The number of Cells will be displayed under "Cells found" and the number of Boards under "Boards found"

The GUI allows you to configure all settings of the AS8506 Chip.

The configuration can be either done via practical dropdown menus on the right-hand side in the **Settings** section or directly to the registers by clicking on **Register Map** and manipulating the registers in a bitwise fashion.

The settings should be pretty self-explanatory but keep in mind to set the correct lower and upper thresholds and reference if you're using the DAC and activate the internal reference and thresholds in the checkboxes to the right:

amu

Upper Threshhold	4,000∨	•	~	internal
Lower Threshhold	3,000V	* *		internal
Reference	3,740V	•	~	internal

Figure 5: Reference and threshold setting

All status information from the boards can by dynamically updated by activating the *Automatic Update* Feature under *Settings*.

This will update ADC values as well as Over-voltage Under-voltage, Zero-cross, and Reference Status Information of each board connected every 2 seconds.

Once the balance process is started update rate will drop to every minute because the chip has to stop its balancing cycle to update the ADC and that should not happen too often.

AS8506 Evaluation Software				
<u>F</u> ile <u>V</u>	iew	<u>S</u> ettings	<u>H</u> elp	
		 Switch 	Trace on	Ctrl+Shift+T
Register	Map	Autom	atic <u>U</u> pdate	Ctrl+U
		<u>E</u> nable	e Chip Detection	Ctrl+Shift+C
Comfo	rtTab			

Figure 6: Automatic Update Feature

Also the *Enable Chip Detection* checkbox allows you to detect when AS8506 Boards have been unplugged from the Interface and reconnected.

Last but not least the ^{Balance} Button allows you to activate the balance feature at will. Green button means balance is active. Gray means not active.

Balance Done LED will light green as soon as the balance process has finished and Cell Voltage or Temp not OK Led will light if the batteries exceed the set boundary limits.



In addition to this Tab there is a graphing tab which gives a graphical representation of the cell voltages and allows you to log the measured voltages to a file.

AS8506 Evaluation Software			
<u>F</u> ile <u>V</u> iew <u>S</u> ettings <u>H</u> elp			
Register Map Readout Registers Balance			amu
ComfortTab GraphTab			
Log to File Autoscale			
3,82			Cell: 1 Cell: 2
3,8			Cell: 3 Cell: 4 Cell: 5 Cell: 6 Cell: 6
3,78			Cell: 7 Cell: 8 Cell: 9 Cell: 10
3,76			Cell: 11 - Cell: 12 - Cell: 13 - Cell: 13 -
3,74			
3,72			
3,7	D4:44 09:	09:0 04:46	4:48
			USB AS8506 (v0.1.2)

Figure 7: Graphing Tab

The *Log to File* button will open a file dialog which selects where the .csv log file will be saved. From then on data that is acquired via the auto update function will automatically be logged to that file.

The *Autoscale* checkbox will automatically zoom in on the cell data. Also the window can be zoomed with the mouse wheel and moved with the left mouse button.







Figure 8: Schematic





Figure 9: Top Layer



Figure 10: Bottom Layer



			1			
	Bill of Mat	erials	AS8506 Demo			
	Company:		ams AG			
	Originator:		GHEH			
	DCB Name		AS9506 Domo			
-	PCD Name.		AS0500 Demo			
_	PCB Version:		0.4			
-	Report Date:		12.12.2012			
#	Designator	Comment	ame Error Component	Manufacturer	Manufacturer Part Number	Quantity
1	C4	4.7uF		MURATA	GRM21BR71A475KA73L	1
2	C5	100nF		KEMET	C0603C104K5RACTU	1
3	C10	100nF		KEMET	C0603C104K5RACTU	1
4	C11	22uF		MULTICOMP	MCCA000555	1
5	D1	SUP Diode		AVX	VC080514A300DP	1
6	D2	ZLLS1000TA		DIODES INC.	ZLLS1000	1
7	D3	ZLLS1000TA		DIODES INC.	ZLLS1000	1
8	J1	BAT				1
9	J2	TOP				1
10	J3	BOTTOM		141 70010	0010400 0441 04 550	1
11	J4	AMS-HUMI		MULTICOMP	600019S-341N-B1-FEC	1
12	JD 01			DIODES INC	2XM0407E	1
13	R1			BOURNS	CR0603-1/-000ELE	1
15	R2	0B		BOURNS	CR0603-1/-000ELF	1
16	R3	0R		BOURNS	CR0603-J/-000ELF	1
17	R4	0R		BOURNS	CR0603-J/-000ELF	1
18	R5	0R		BOURNS	CR0603-J/-000ELF	1
19	R7	0R		BOURNS	CR0603-J/-000ELF	1
20	R8	0R		BOURNS	CR0603-J/-000ELF	1
21	R9	0R				1
22	R10	0R		BOURNS	CR0603-J/-000ELF	1
23	R11	0R				1
24	R12	0R		BOURNS	CR0603-J/-000ELF	1
25	R13	300K 0.1%				1
26	R14	100K 0.1%		TE CONNECTIVITY	RP/3PF2A100KBTDF	1
27	R15			PANASUNIC	CR0602 // 000ELE	1
28	R17	0R		BOURNS	CR06031/-000ELF	1
30	R18	OR		000.040	CI DOGG DI-DUDELI	1
31	R19	0R		BOURNS	CR0603-J/-000ELF	1
32	R21	0R				1
33	R22	12R		MULTICOMP	MCHP06W2F120JT5E	1
34	R23	0R				1
35	R24	0R		BOURNS	CR0603-J/-000ELF	1
36	R25	470R		VISHAY DRALORIC	CRCW0603470RFKEA	1
37	R26	0R		BOURNS	CR0603-J/-000ELF	1
38	T1	WE-FLEX 749196111				1
39	01	A S8506			4 CD 1 1000	1
40	03			AVAGO TECHNOLOGIES	ACHL-M/21-000E	1
41	04 avad	74ATC16004	Noton		74A HC 16004679/11	41
Appr	oved		Notes			41
-						
-						
-						

Figure 11: BOM



7 Ordering Information

The AS8605 Passive Balancer demo can be ordered via:

Table 4: Ordering Information

Ordering Code	Productname	Materialnumber
AS8506-DK-PASSIVE	AS8506 Passive Balancer Board	990600767

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