Product data sheet

1 General description

The 74LVT08 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

The 74LVT08 is a quad 2-input AND gate.

2 Features and benefits

- Wide supply voltage range from 2.7 V to 3.6 V
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Latch-up protection
 - JESD78 Class II exceeds 500 mA
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

3 Ordering information

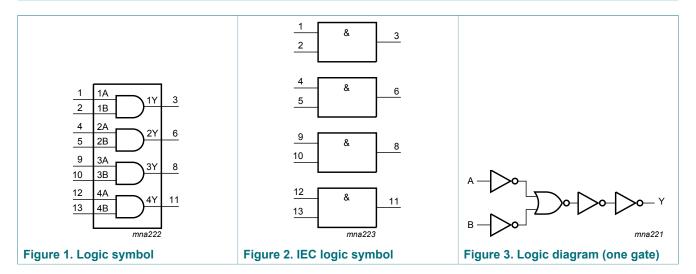
Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
74LVT08D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1			
74LVT08DB	-40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1			
74LVT08PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1			



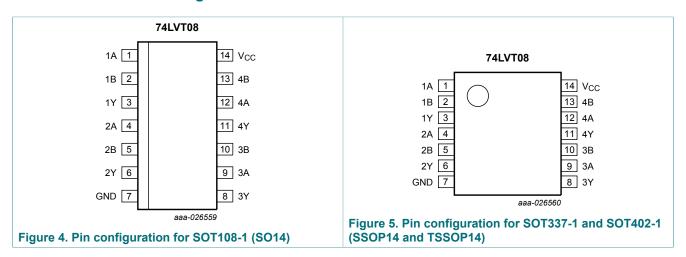
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4 Functional diagram



5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

able 2. Fill description						
Symbol	Pin	Description				
1Y to 4Y	3, 6, 8, 11	data output				
1A to 4A	1, 4, 9, 12	data input				
1B to 4B	2, 5, 10, 13	data input				
GND	7	ground (0 V)				
V _{CC}	14	supply voltage				

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6 Functional description

Table 3. Function table [1]

Input	Output	
nA	nB	nY
Н	Н	Н
Н	L	L
L	Н	L
L	L	L

^[1] H = HIGH voltage level; L = LOW voltage level

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
VI	input voltage	[1]	-0.5	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
Io	output current	output in LOW-state	-	64	mA
		output in HIGH-state	-32	-	mA
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[2]	-	150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 \text{ to } +85 ^{\circ}\text{C}$ [3]	-	500	mW

^[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8 Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
VI	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-20	-	-	mA
I _{OL}	LOW-level output current		-	-	32	mA

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^[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

^[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K. For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb}	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

Static characteristics 9

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T _{amb} = -4	0 °C to +85 °C				ı	
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2		-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output	V_{CC} = 2.7 V to 3.6 V; I_{OH} = -100 μA	V _{CC} - 0.2		-	V
	voltage	V _{CC} = 2.7 V; I _{OH} = -6 mA	2.4	-	-	V
		V _{CC} = 3.0 V; I _{OH} = -20 mA	2.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 μ A	-		0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-		0.5	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-		0.5	V
I _I	input leakage current	V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	-	10	μΑ
		V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	±1	μA
l _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 0 \text{ V to } 4.5 \text{ V}$			±100	μA
I _{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC} ; I_O = 0 A				
		output HIGH	-	-	0.02	mA
		output LOW	-	1	2	mA
ΔI _{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input at V_{CC} - 0.6 V and other inputs at V_{CC} or GND	[2] _		0.2	μA
C _I	input capacitance	V _I = 0 V or 3.0 V	-	4	-	pF
Co	output capacitance	V _O = 0 V or 3.0 V	-	10	-	pF

Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

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10 Dynamic characteristics

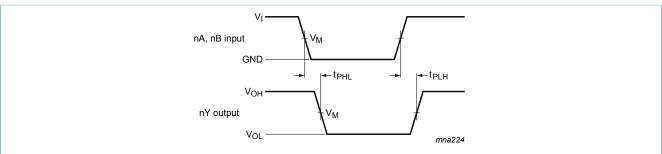
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T _{amb} = -40	0 °C to +85 °C					
t _{PLH}	LOW to HIGH	nA or nB to nY; see Figure 6				
	propagation delay	V _{CC} = 2.7 V	-	-	4.7	ns
		V _{CC} = 3.0 V to 3.6 V	1	3.0	3.9	ns
t _{PHL}	HIGH to LOW	nA or nB to nY; see Figure 6				
	propagation delay	V _{CC} = 2.7 V	-	-	4.8	ns
		V _{CC} = 3.0 V to 3.6 V	1	3.4	4.6	ns

^[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

10.1 Waveforms and test circuit



Measurement points are given in <u>Table 8</u>.

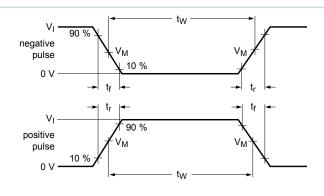
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

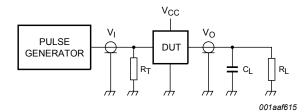
Figure 6. Propagation delay input (nA, nB) to output (nY)

Table 8. Measurement points

Input	Output		
V _M	V _I	V _M	
1.5 V	2.7 V	1.5 V	

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Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

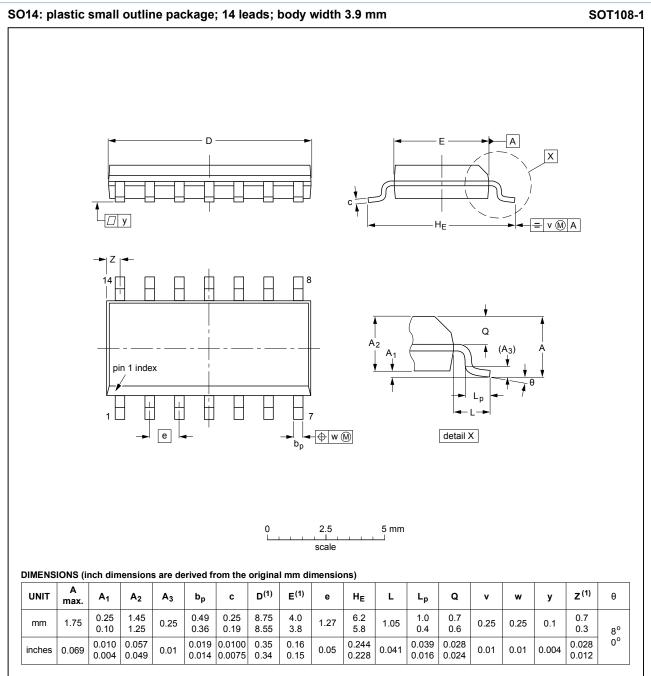
R_L = load resistance.

Figure 7. Test circuit for measuring switching times

Table 9. Test data

Input			Load		Test	
VI	fi	t _W	t _r , t _f	CL	R _L	
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	t _{PLH} , t _{PHL}

11 Package outline



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	REFERENCES EUROPEAN		ICCUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

Figure 8. Package outline SOT108-1 (SO14)

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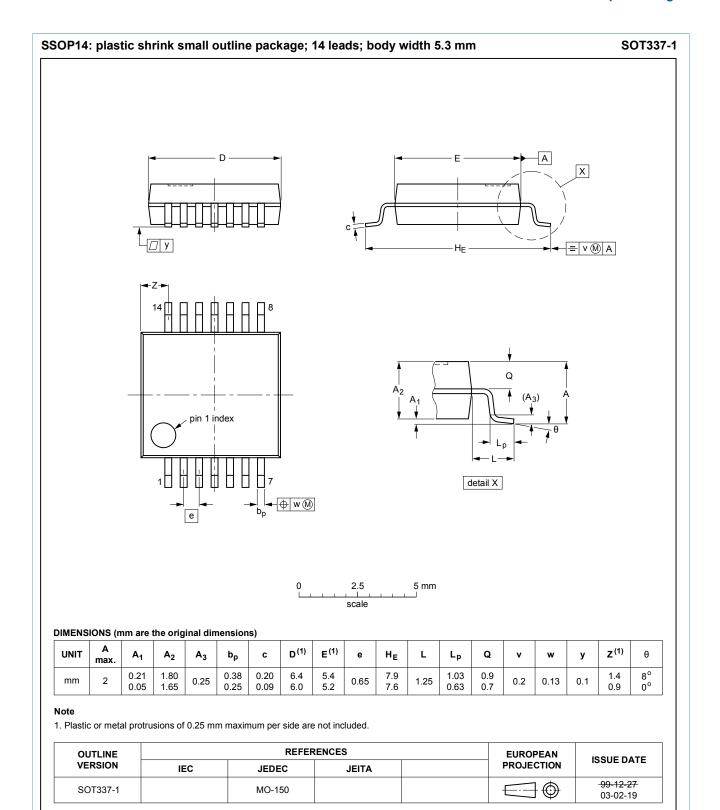
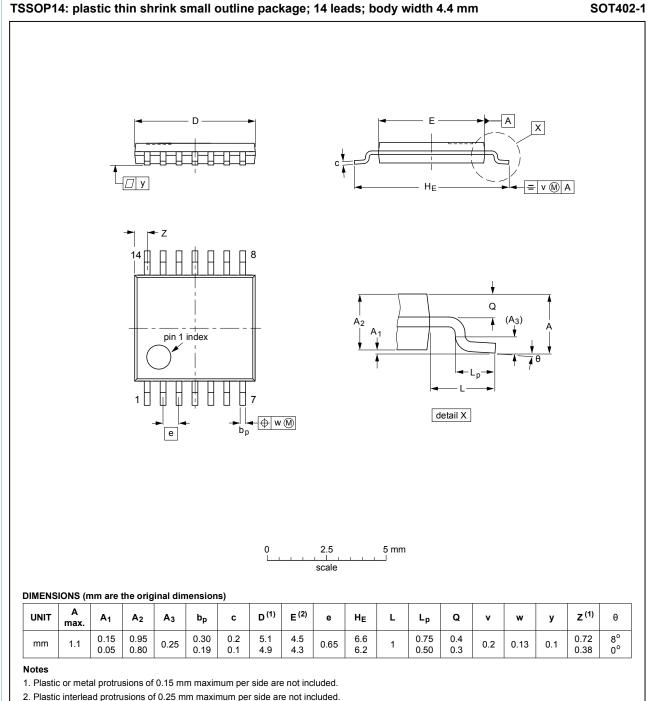


Figure 9. Package outline SOT337-1 (SSOP14)

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	OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSIC	VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
	SOT402-1		MO-153			99-12-27 03-02-18

Figure 10. .Package outline SOT402-1 (TSSOP14)

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12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74LVT08 v.3	20170322	Product data sheet	-	74LVT08 v.2		
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 					
74LVT08 v.2	19960529	Product specification	-	74LVT08 v.1		

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14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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