PIC18F2480/2580/4480/4580 Rev. A1 Silicon Errata

The PIC18F2480/2580/4480/4580 Rev. A1 parts you have received conform functionally to the Device Data Sheet (DS39637**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2480/2580/4480/4580 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F2480/2580/4480/4580 silicon.

The following silicon errata apply only to PIC18F2480/2580/4480/4580 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2480	01 1010 100	00001
PIC18F2580	01 1010 110	00001
PIC18F4480	01 1010 101	00001
PIC18F4580	01 1010 100	00001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: ECCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the ECCP in Compare mode with the Special Event Trigger (CCP1CON bits, CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F458, where the Special Event Trigger Reset of the timer occurs on the next rollover of the prescale counter, after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period on the PIC18F4580 family as the PIC18F458 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F458, to achieve the same Reset period on the PIC18F4580 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 (depending on the T1CKPS1:T1CKPS0 bit values).

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a reset of the Baud Rate Generator which will effect any ongoing transmission.

Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H was written. It does not change the actual prescale value.

Work around

Do not write to TMR1H/TMR3H while Timer1/Timer3 is running, or else write to TMR1L/TMR3L immediately following a write to TMR1H/TMR3H.

Do not write to TMR1H/TMR3H and then wait for another event before also updating TMR1L/TMR3L.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Interrupts

If an interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register. Upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction "`MOVFF TEMP, WREG`" the `MOVFF` instruction will be completed and WREG will be loaded with the value of `TEMP` before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where `Fd` is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where `Fd` is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

Work around

1. Assembly Language Programming:

   If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save and then restore WREG, BSR and STATUS via software as shown in Example 8-1 in the Device Data Sheet.

   Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead. For example, use:

   ```
   MOVF   TEMP, W
   MOVWF  BSR
   ```

   instead of `MOVFF TEMP, BSR`.

   As another alternative, the following work around shown in Example 1 can be used. This example overwrites the Fast Return register by making a dummy call to `Foo` with the fast option in the high priority service routine.

EXAMPLE 1: ASSEMBLY LANGUAGE INTERRUPT SERVICE

```
ISR @ 0x0008
    CALL       Foo, FAST  ; store current value of WREG, BSR, STATUS for a second time
Foo:
    POP                   ; clears return address of Foo call
    :                     ; insert high priority ISR code here
    :
    RETFIE     FAST
```

2. C Language Programming:

   The exact work around depends on the compiler in use. Please refer to your C compiler documentation for details.

   If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as "low priority" by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

The code segment, shown in Example 2, demonstrates the work around using the C18 compiler.

EXAMPLE 2: INTERRUPT SERVICE ROUTINE IN C

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

An optimized C18 version, which illustrates how to reduce the instruction cycle count to 3, is provided in Example 3.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 3: OPTIMIZED INTERRUPT SERVICE ROUTINE

```
#pragma code high_vector_section=0x8
void high_vector (void)
{
  _asm
    CALL high_vector_branch, 1
  _endasm
}

void high_vector_branch (void)
{
  _asm
    POP
    GOTO high_isr
  _endasm
}

#pragma interrupt high_isr
void high_isr (void)
{
  ...
}
```

5. Module: ECAN™ Technology

Under specific conditions, the first five bits of a transmitted identifier may not match the value in the Transmit Buffer ID register, TXBnSIDH. The following conditions must exist for the corruption to occur:

1. A transmit message must be pending.
2. The ECAN module must detect a Start-of-Frame (SOF) in the third bit of interframe space.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: ECAN™ Technology

The Error Interrupt Flag, ERRIF (PIR3<5>), may not be able to clear in software after either of the following counter registers exceeds 127.

- Transmit Error Counter Register TXERRCNT
- Receive Error Counter Register RXERRCNT

Work around

Monitor the EWARN (COMSTAT<0>) bit to determine if either the TXERRCNT or the RXERRCNT exceeds 95 and clear the ERRIF flag before either counter reaches 127.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: ECAN™ Technology

Following an error on the bus, the ECAN module is unable to switch from Listen Only mode directly to Configuration mode.

Work around

Use the REQOP (CANCON<7:5>) bits to select Normal mode as an intermediate step when switching from Listen Only mode to Configuration mode.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: ECAN™ Technology

Under specific conditions, the TXBnSIDH register of the pending message for transmission may be corrupted. The following conditions must exist for this event to occur:

1. A transmit message must be pending.
2. All of the receive buffers must be full and a received message is in the Message Assembly Buffer (MAB).
3. A receiver buffer must be made available (RXBxCON<RXFUL> set to '0') when a Start-of-Frame (SOF) is recognized on the CAN bus, or on the instruction cycle prior to the SOF for the TXBxSIDH corruption event to occur. The timing of this event is crucial.

Work around

Ensure that a receive buffer overflow condition does not occur and/or ensure that a transmit request is not pending if a receive buffer overflow condition does exist.

The pseudo-code segment in Example 4 is an example of how to disable a pending transmission. This code is for illustration purposes only.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 4:

```
If (RXBnOVFL == 1)                  // Has an overflow occurred?
    {       If (TXREQ == 1)                 // Is a transmission pending?
            {       TXREQ = 0;              // Clear transmit request
                    If (TXABT == 1)         // Store transmission aborted status value
                            MyFlag = 1;
            }
    }
    Temp_RXREG = RXBx;                      // Read receive buffer
    If (MyFlag)                             // Was previous transmission aborted?
    {       TXREQ = 1;                      // Set transmit request
            MyFlag = 0;                     // Reset stored transmission aborted status
    }
```

9. Module: MSSP

In SPI mode, the SDO output may change after the inactive clock edge of the bit '0' output. This may affect some SPI components that read data over 300 ns after the inactive edge of SCK.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: ECAN™ Technology

In Listen Only mode, the ECAN module may persistently set the IRXIF and RXB0IF interrupt flags and the RXFUL status flag, after receiving 129 or more consecutive error frames. In this case, the flags can be cleared, but then will become set again immediately and continuously without receiving a bus message.

Work around

Place the ECAN module in Configuration mode before receiving 129 consecutive error frames, and then place it back into Listen Only mode.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: 10-Bit Analog-to-Digital Converter

When the AD clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select the AD clock source as 4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC and avoid selecting 2 TOSC or RC.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (11/2004)
Original version of this document. Includes silicon issues 1 (ECCP), 2 (EUSART), 3 (Timer1/Timer3) and 4 (Interrupts).

Rev B Document (12/2006)
Updated silicon issue 4 (Interrupts) to include additional examples in assembly and optimized C; added silicon issues 5 through 8 (ECAN™ Technology) and 9 (MSSP).

Rev C Document (2/2007)
Correct silicon issue 5 (ECAN™ Technology). Corrected code comment in Example 4 for silicon issue 8 (ECAN™ Technology).

Rev D Document (4/2007)
Added silicon issue 10 (ECAN™ Technology).

Rev E Document (5/2007)
Added silicon issue 11 (10-Bit Analog-to-Digital Converter).

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