Freescale Semiconductor

Advance Information

Document Number: MC33285 Rev. 5.0, 2/2007

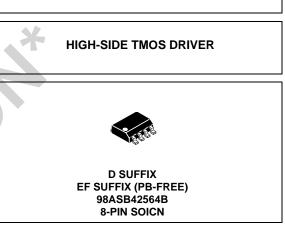
Dual High-Side TMOS Driver

A single input controls the 33285 in driving two external high-side N-Channel TMOS power FETs controlling incandescent or inductive loads. Pulse Width Modulated (PWM) input control to 1.0 kHz is possible. The 33285 contains a common internal charge pump used to enhance the Gate voltage of both FETs.

An external charge capacitor provides access to the charge pump output. Both external FETs are protected against inductive load transients by separate internal source-to-gate dynamic clamps. The power FETs are protected by the 33285 with short-circuit delay time of 800 µs. The device is designed to withstand reverse polarity battery and load dump transients, encountered in automotive applications.

Features

- PWM Capability
- Power TMOS Number One (OUT1) Short-Circuit Detection and Short-Circuit Protection
- Voltage Range 7.0 V \leq 40 V
- Extended Temperature Range from -40°C ≤ 125°C
- Load Dump Protected
- Overvoltage Detection and Activation of OUT2 During
 Overvoltage
- Single Input Control for Both Output Stages
- Capacitor Value of 100 nF Connected to Pin CP
- Analog Input Control Measurement Detection
- OUT1 LOAD Leakage Measurement Detection
- Pb-Free Packaging Designated by Suffix Code EF



33285

ORDERING INFORMATION

Device	Temperature Range (T _A)	Package
MC33285D/R2	-40°C to 125°C	8 SOICN
MCZ33285EF/R2	-40 0 10 125 0	0.0000

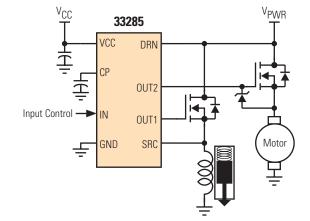


Figure 1. 33285 Simplified Application Diagram

* This document contains certain information on a new product.
 Specifications and information herein are subject to change without notice.
 © Freescale Semiconductor, Inc., 2007. All rights reserved.



INTERNAL BLOCK DIAGRAM

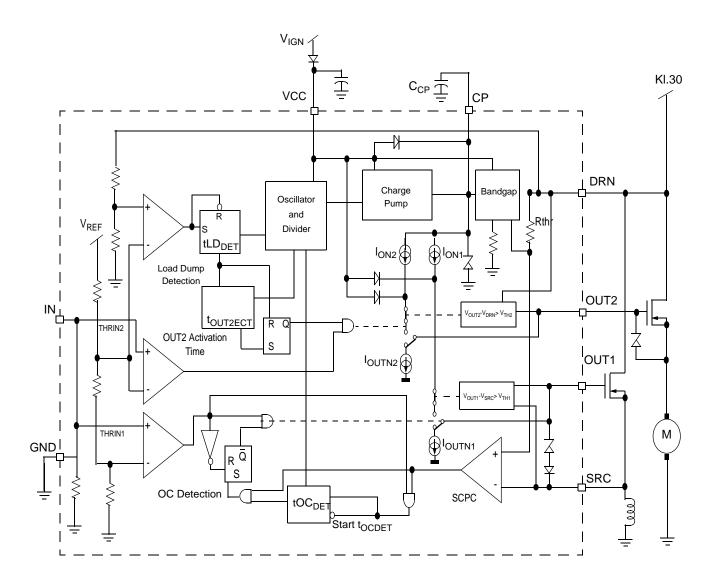


Figure 2. 33285 Simplified Internal Block and Typical Applications Diagram

PIN CONNECTIONS

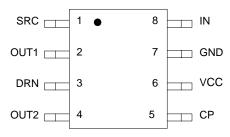




Table 1. 33285 Pin Definitions

Pin Number	Pin Name	Formal Name	Definition
1	SRC	Source	OUT2 external FET Source connection
2	OUT1	Output 1	This pin is output number 1
3	DRN	Drain	OUT1 and OUT2 external FET Drain connection
4	OUT2	Output 2	This pin is output number 2
5	СР	Charge Pump	External capacitor connection for internal the Charge Pump
6	VCC	Voltage Power Supply	Battery supply voltage
7	GND	Ground	This is the ground pin.
8	IN	Input	Voltage level sensitive input for OUT1 and OUT2

ELECTRICAL CHARACTERISTICS MAXIMUM RATINGS

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			1
Maximum Voltage at Pins OUT1 and OUT2	V _{OUT}	V _{VCC} + 20	V
Maximum Voltage at Pin CP	V _{CP}	50	V
Input Voltage V _I at DRN	V _{DRN}	-2.0 to 40	V
Input Voltage V _I at SRC	V _{SRC}	-5.0 to 40	V
Input Voltage at Pin VCC	V _{CC}	-2.0 to 40	v
Input Voltage at Pin IN. Condition: -2.0 V < V _{VCC} < 40 V	V _{IN}	-2.0 to V _{VCC}	V
Operational Voltage V _{VCC} at Pin VCC	V _{VCC}	7.0 to V _I	V

Storage Temperature	T _{STG}	-40 to150	°C
Operating Ambient Temperature	T _A	-40 to 125	°C
Peak Package Reflow Temperature During Reflow ⁽¹⁾ , ⁽²⁾	T _{PPRT}	Note 2	°C

Notes

1. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

 Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions T_A from -40°C \leq 125°C, V_{CC} from 7 V \leq 20 V, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25$ °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
OVERVOLTAGE AND OVER CURRENT					
Load Dump Activation Time	t _{OUT2ACT}	300	460	620	ms
Error Voltage Threshold	V _{DRN} - V _{SRC}	1.12	_	1.44	V
SRC PIN 1	-++			• •	
Leakage Current	ILC _{DET}	15	30	50	mA
Leakage Current Detection Time	tLC _{DET}	130	200	270	μA
DRN PIN 3					
Operating Current (7.0 V < V _{DRN} < 20 V)	I _{DRN}	_	—	1.5	mA
Leakage Current (0 V < V_{DRN} < 20 V, V_{VCC} < 4.0 V)	I _{LEAK-DRN}	-5.0	_	5.0	μA
OUT1, PIN 2, AND OUT2 PIN 4					
Output ON Voltage. Charge Pump ON	V _{ON}	_	—	V _{CC} + 15	V
Turn OFF Current, V _{OUT} > 0.5 V	IOUTOFF	66	110	154	μA
V _{CC} PIN 6					
Supply Voltage Range	V _{CC}	7.0	_	40	V
Quiescent Supply Current at V_{CC} = 20 V	I _{CC}	_	_	10	mA
IN PIN 8					
Input Low Voltage OUT1	V _{IL}	_	—	0.7	V
Input High Voltage OUT1	VIH	1.7	_	—	V
Input Hysteresis OUT1 and OUT2	V _{HYS}	0.4	_	—	V
Input Pull Down Current, 0.7 V < V _{IN} < 6.0 V	I _{IN}	7.5	15	16.5	μA
Open Input Voltage	V _{IOP}	_		0.7	V
Input Low Voltage OUT2	V _{IL2}	_	_	3.0	V
Input High Voltage OUT2	V _{IH2}	3.9		_	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions T_A from -40°C \leq 125°C, V_{CC} from 7 V \leq 20 V, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

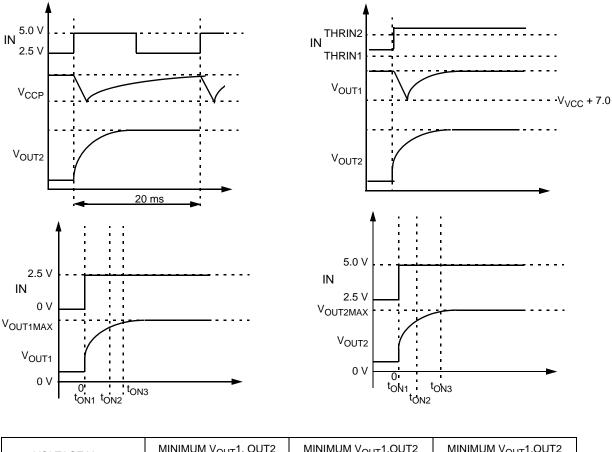
Characteristic	Symbol	Min	Тур	Max	Unit
OVER VOLTAGE AND OVER CURRENT					
Load Dump Detection Time	tLD _{DET}	250	400	550	μs
Over Current Detection Time	tOC _{DET}	520	800	1080	μs
OUT1 PIN 2, AND OUT2 PIN 4					
Turn ON Time, OUT1: 8.0 nF, 10 μA; OUT2:16 nF, 10 μA	t _{ON}	_	_		ms
-7.0 V < V_{CC} < 10 V, V_{OUT} > V_{CC} + 7.0		—	—	1.5	
-10 V < V _{CC} < 20 V, V _{OUT} > V _{CC} + 11				1.5	

FUNCTIONAL DESCRIPTION

INTRODUCTION

The power FETs are turned ON by charging their gate capacities with a current flowing out of pins OUT1 and OUT2. During PWM, the values of table below are guaranteed. They

are measured with 8.0 nF on OUT1 and 16 nF on OUT2. Test condition V_{IN}: ramp 0 V \leq 2.5 V or 2.5 V \leq 5.0 V.



VOLTAGE V _{VCC}	MINIMUM V _{OUT} 1, OUT2	MINIMUM V _{OUT} 1,OUT2	MINIMUM V _{OUT} 1,OUT2
	AFTER T _{ON1} = 100 µSEC	AFTER T _{ON2} = 1.0 µSEC	AFTER T _{ON3} = 1.5 μSEC
7.0 V < V _{VCC} < 10 V 10 V < V _{VCC} < 20 V 20 V < V _{VCC} < 40 V	V _{VCC} - 0.7 V V _{VCC} - 0.7 V V _{VCC} - 0.7 V	V _{VCC} + 5.95 V V _{VCC} + 9.35 V	V _{VCC} + 7.0 V V _{VCC} + 11 V

Figure 4. Turn On Behavior

Turn Off Characteristics

The output voltages at OUT1 and OUT2 are limited by controlling the current sources $I_{ON1},\,I_{ON2}$ to avoid current flowing through the external or the internal zener diode.

When voltage power supply plus threshold voltage (V_{CC} + V_{TH}) is reached, the current sources are turned OFF.

- Threshold V_{TH1} for OUT1 output voltage control is 7.0 V < V_{TH1} < V_Z
- Threshold V_{TH2} for OUT2 output voltage control is 7.0 V < V_{TH2} < 15 V

The power FETs on OUT1 and OUT2 are turned OFF by discharging the gate capacity with the constant discharge current I_{OUTOFF} .

- Discharge current $I_{OUTxOFF}$ is $I_{OUTxOFF}$ = 110 μA condition: $V_{OUT}\,x$ > 0.5 V (V_{IN} < V_{THRxIN})
- Test conditions for switching OFF the power FETs:
 - 1. IN open
 - 2. Stages disabled via pin IN
 - 3. Stage OUT1 disabled by an over current error

33285

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

INTRODUCTION

The 33285 contains only one charge pump for two outputs. The outputs, OUT1 and OUT2, are switched ON and OFF by the input (IN) .There are three ways to control the outputs:

OUT1 can be switched alone

OUT1 and OUT2 can be switched together

OUT2 can be switched when OUT1 is already on

In the last case, the voltage drop on OUT1 when charging OUT2 is limited.

The external capacitor (C_{CP}) connected to the CHARGE PUMP (CP) pin is used to store the charge continuously delivered by the charge pump. The voltage on this pin is limited to a maximum value V_{CPMAX}. Both outputs are sourced with a constant current from C_{CP} to switch them ON. Additionally, the gates of the power FETs are precharged from voltage power supply (V_{CC}) to prevent C_{CP} from being discharged by a voltage on OUT1 or OUT2, is still lower than V_{VCC}. The values of the output voltages are limited to V_{OUT1MAX} and V_{OUT2MAX}.

The power FET on OUT1 is protected against an exceeded gate-source voltage by an internal zener diode.

Channel One protects the N-Channel power FET on OUT1 undercurrent and short-circuit conditions. The drain-source voltage of the FET on OUT1 is checked if Channel One is switched ON. The internal error voltage threshold determines the maximum drain-source voltage allowing the power FET to stay in the ON state. If the measured drain-source voltage exceeds the internal error voltage threshold, the output of the short-circuit protection comparator (SCPC) is enabled. If the output of the SCPC is active longer than t_{OCDET}, output OUT1 is switched OFF.

After switching OFF the power FET on OUT1 by an shortcircuit condition, the power FET can only be turned ON again by the input IN.

When switching OFF the power FETs their gate capacities are discharged by a constant current, I_{OUTOFF} .

If the input IN is disconnected, the 33285 outputs, OUT1 and OUT2, are in the OFF state.

If overvoltage occurs on the DRAIN (DRN) pin for a time period longer than t_{LDDET} , OUT2 is switched ON for the time $t_{OUT2ACT}$. In an overvoltage condition OUT1 is OFF if IN is below V_{IH} .

INTERNAL ZENER DIODE

An on-chip zener diode is placed between OUT1 and The SOURCE (SRC). Design guarantees $V_Z > V_{TH1}$. Zener clamping voltage between OUT1 and SRC is $V_{TH1} < V_Z < 20 \text{ V}$

PWM CAPABILITY

The C_{PIC2} is PWM capable on OUT2. The loss of charge ON C_{CP} when switching ON OUT2 is refreshed until the Start on the next PWM cycle to a value sufficient to guarantee the specified turn ON behavior.

The PWM capability is measured with a test circuit and load conditions:

- PWM cycle is period T = 20 ms; OUT2 is switched ON from 10 to 90 percent of T
- Test condition V $_{I\!N}$ ramps 2.5 V \leq 5.0 V according to PWM cycle defined above

CROSS TALK BETWEEN OUT1 AND OUT2

If output OUT2 is switched ON while OUT1 is already ON, the voltage drop occurring on OUT1 is limited.

Voltage drop on OUT1:

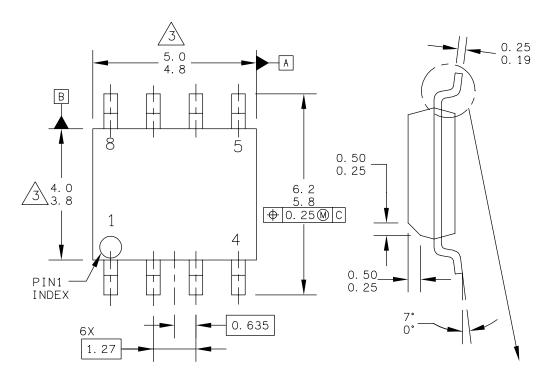
- 10 V < V_{VCC} < 20 V : OUT1 not below V_{VCC} + 7.0 V
- 7.0 V < V_{VCC} < 20 V : OUT1 not below V_{VCC} + 7.0 V

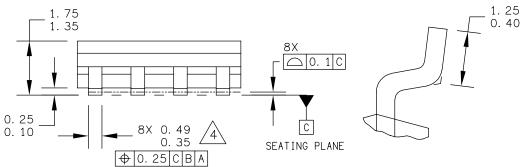
Each time OUT1 is switched ON, a current I_{LCDET} is sourced out of the SRC pin for the time t_{LCDET} to check if there is an external leakage current on that node in the application. The high-side switch on OUT1 is turned ON only if the test is successful.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit <u>www.freescale.com</u> and perform a keyword search using the "98A" listed below.





© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE:		DOCUMENT NO	: 98ASB42564B	REV: U
8LD SOIC NARROW	8LD SOIC NARROW BODY		: 751–07	07 APR 2005
		STANDARD: JE	DEC MS-012AA	

D SUFFIX EF SUFFIX (PB-FREE) PLASTIC PACKAGE 98ASB42564B ISSUE U

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	9/2006	 Implemented Revision History page Converted to Freescale format Added part number MCZ33285EF (Pb-FREE) to Ordering Information
5.0	2/2007	 Added Peak Package Reflow Temperature During Reflow ⁽¹⁾, ⁽²⁾ to Maximum Ratings Added notes ⁽¹⁾ and ⁽²⁾

REVISION HISTORY

How to Reach Us:

Home Page: www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor Technical Information Center, CH370 1300 N. Alma School Road Chandler, Arizona 85224 +1-800-521-6274 or +1-480-768-2130 support@freescale.com

Europe, Middle East, and Africa: Freescale Halbleiter Deutschland GmbH

Freescale Halbleiter Deutschland G Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd. Technical Information Center 2 Dai King Street Tai Po Industrial Estate Tai Po, N.T., Hong Kong +800 2666 8080 support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center P.O. Box 5405 Denver, Colorado 80217 1-800-441-2447 or 303-675-2140 Fax: 303-675-2150 LDCForFreescaleSemiconductor@hibbertgroup.com RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to http:// www.freescale.com/epp.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale[™] and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc., 2007. All rights reserved.



MC33285 Rev. 5.0 2/2007