xCORE-200 sliceKIT Hardware Manual

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XMOS

SYNOPSIS

This document pertains to the 1V1 revision of the xCORE-200 sliceKIT General purpose XL Board.

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1 Overview

IN THIS CHAPTER

This document covers the hardware design of the xCORE-200 General Purpose sliceKIT Core Board (Part#: XP-SKC-XL216).

The Core Board contains a fully pinned out 500MHz, 16-core XL216-512-FB236 device, with its GPIOs connected to three expansion connectors (termed Slots) to interface with expansion cards (called sliceCARDs) that plug into the slots. The Core Board contains all circuitry necessary for operating and debugging the XMOS system. Multiple sliceKIT Core Boards can be interconnected to form a multi XMOS device system with bi-directional 5-bit xCONNECT Links being present between the boards. The xCORE-200 General Purpose Core Board is only capable of being the start of a chain i.e. the chain master.

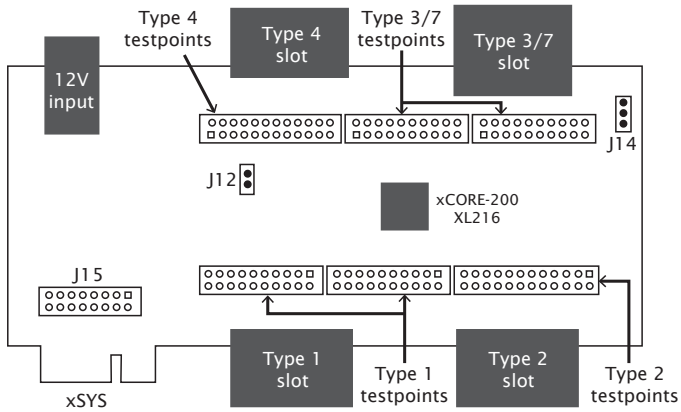

Figure 1: xCORE-200 General Purpose(XL) sliceKIT Core Board - Block diagram

1.1 Main features

- 500MHz xCORE-200 Device XL216-512-FB236
- 16 real-time logical cores on two xCORE tiles
- 128 user configurable GPIOs
- On-board 25MHz clock
- Advanced Debug Support - JTAG and xCONNECT Interfaces
- Backward compatibility to older sliceCARDs
- Higher memory capacity (Internal and External)
- xSYS interface and xCONNECT Link interfaces for system expansion

1.1.1 Slot naming conventions

xCORE-200 devices like the XL216-512-FB236 used on the xCORE-200 sliceKIT Core Board, include dedicated 32 bit ports in addition to the 1, 4, 8 and 16 bit ports supported on XS1 sliceKIT Core Boards. To support the additional ports, a numeric naming convention is used on xCORE-200 sliceKIT Core Boards instead of the symbols used previously. The following table shows the new and old conventions.

XS1 Symbol	xCORE-200 Number	Description
U	U	USB
A	A	Analog
STAR	1	1, 4, 8, 16-bit ports
TRIANGLE	2	1, 4, 8, 16-bit ports
SQUARE	3	1, 4, 8, 16-bit ports
CIRCLE	4	1, 4, 8, 16-bit ports
DIAMOND	5	1, 4, 8, 16-bit ports
-New-	6	32-bit ports
-New-	7	32-bit ports

2 Hardware

IN THIS CHAPTER

2.1 xCORE-200 Microcontroller

The xCORE-200 General Purpose Core Board includes the XL216-512-FB236 device and support circuitry. The device GPIO are connected to the Slots, with test points available for each signal.

The Core Board is powered by a 12V external power supply, provided with the kit.

An xTAG debug adapter can be connected to the xSYS connector, providing a debug link from a USB host.

2.2 Power

Power input to the sliceKIT core board is via a standard barrel jack connector. A standard 12V external power supply should be used to power the board. Each core board requires its own 12V supply. This input supply is used to generate the main 5V board supply via a DC-DC converter.

The 5V board supply is then fed to all the slot connectors as well as powering the core board itself. 3V3 and 1V0 supplies are be generated by DC-DC converters from the 5V main supply. The supplies are sequenced to ensure the power up sequence is 5V then 3V3 then 1V0. When the 1V0 supply is good, the system is released from reset.

The core board provides 3V3 and 5V at 0.25A each for a total of approximately 2W per slice.

2.3 Clock

The system clock has two sources: an on-board 25MHz oscillator or the CLK signal from the Chain connector. The system clock source is selected automatically according to the Master Present signal on the Chain connector. The 25MHz clock is used as reference clock at the start of chain and would be used as system clock.

The system clock from a Master Core Board is fed automatically to all of the slave Core Boards so the whole system will operate synchronously.It is also fed to each of the sliceCARD slots.

2.4 JTAG and xSYS Interface

Debug of the system is via the xSYS Connector on the plug chain connector.

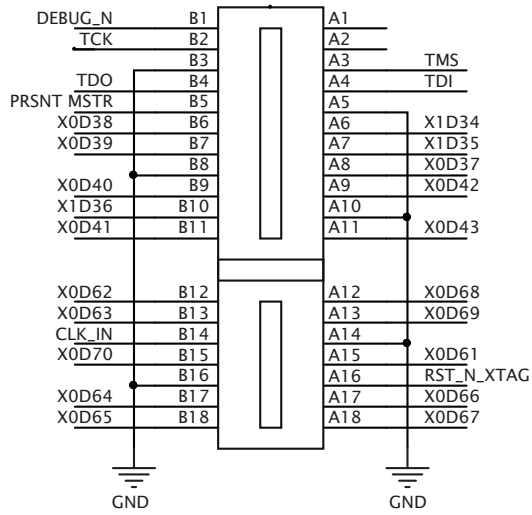

Figure 2: sliceKIT plug chain connector

A Master Present signal is present on Type-7 Slot connector to allow detection of a connected board and subsequent automatic switching of the JTAG chain. In a system of multiple Core Boards, the Master is the source of the JTAG chain so the system can only be debugged from the master. Other boards will see no devices in the JTAG chain.

The xSCOPE xCONNECT link can be either enabled or disabled via a switch on the xTAG adapter board labelled xLINK. The Type-3 slot contains two 5-bit xCONNECT Links, XL1 and XL2, which can be used for chaining sliceKIT Core Boards together.

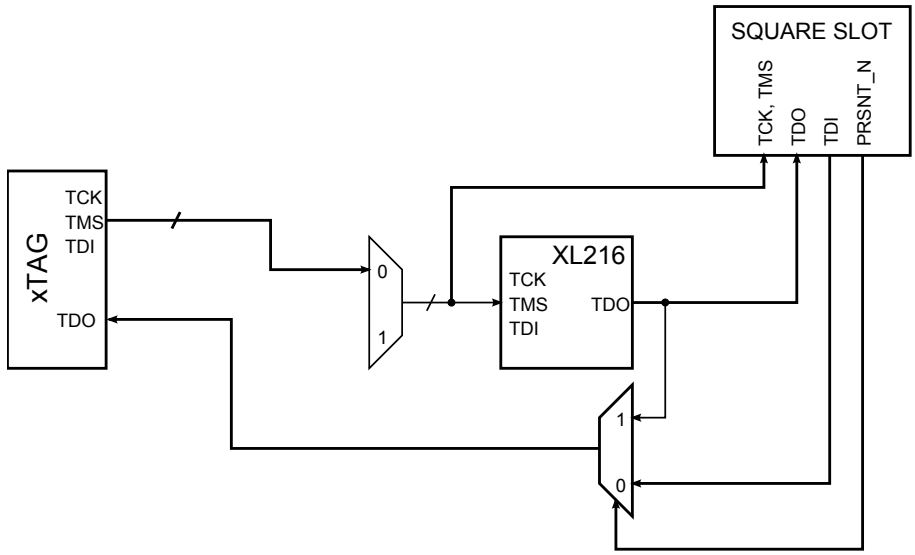

Figure 3: sliceKIT JTAG chain flow diagram

2.5 xCORE-200 device boot

sliceKIT includes 2MB onboard Quad-SPI flash for storage requirements. Master Core Boards boot from QSPI flash, while slave Core Boards boot from xCONNECT link `XL0` from the next connected Core Board.

The switching is controlled by X0D32 and X0D33. Once the device has booted X0D32 is used to enable or disable the QSPI interface, X0D33 should then transition from low to high to latch the selection. The QSPI selection state is then maintained until the system is reset.

Once this sequence is completed the selection has been latched therefore X0D32 and X0D33 return to performing their normal functions in the respective slots. To allow re-use of the QSPI boot pins (ports 1B, 1C and 4B) as GPIO pins, a jumper provision - J12 is used which connects the xCORE QSPI pins to either the QSPI Flash or to the sliceCARD Slots.

If the SPI is not disabled, then sliceCARDs in the‘‘Type-2‘‘ slots may not function as expected. If there are no sliceCARDs in the `Type-2` slot, then it does not matter whether the QSPI has been disabled or not. Therefore, applications which require runtime access to the QSPI flash should either leave the `Type-2` slot unpopulated or check to ensure that the Card(s) which are in there will be unaffected by the operation of the Flash.

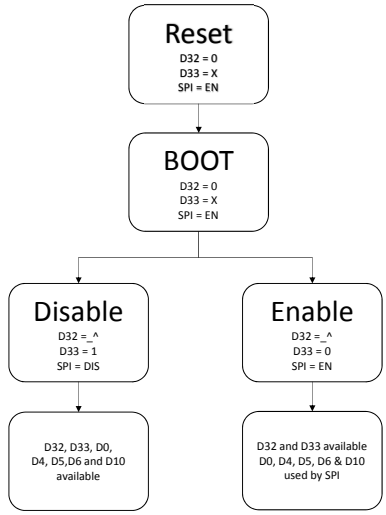

Figure 4: QSPI Select Flow Diagram

The xTAG debug adapter system can use the boot mode select signal to force all devices in the chain (master and slave Core Boards) to boot from JTAG (don't boot) for debug purposes.

If not in this mode, devices boot from QSPI or xCONNECT link as appropriate.

2.6 xCONNECT Links

The Type-7 slot contains two 5-bit xCONNECT Links, XL1 and XL2, which can be used for chaining sliceKIT Core Boards together.

To boot systems with more than one core board chained by xCONNECT links, the links must have a delay of four clock cycles or more. This can be configured in the XN file, for example:

```
<Link Encoding = "5wire" Delays="4,4" >
```

To boot a slave board in a chain, jumper J14 must be in the 2-3 position, to enable pins that have xCONNECT Link 6. There is no link to a slave board with J14 in 1-2 position.

2.7 Reset

The whole system is held in reset until all power supplies are stable, and reset is connected to all sliceCARDs so any circuitry on them can be reset.

It also indicates to the sliceCARDs that their power input is stable. The reset from the xTAG debug adapter resets the whole system, if required for debugging.

2.8 Slots - Signals List

2.8.1 Type-1 Slot - Pinout table-Top side

PCIE TOP	SIGNAL	FUNCTION				
B1	NC	No connection				
B2	NC	No connection				
B3	GND	Ground				
B4	NC	No connection				
B5	3.3V	+3.3V Voltage rail				
B6	X0D02		4A0	8A0	16A0	32A20
B7	X0D03		4A1	8A1	16A1	32A21
B8	GND	Ground				
B9	X0D04		4B0	8A2	16A2	32A22
B10	X0D10_EXT	XL33out 1C0				
B11	X0D05		4B1	8A3	16A3	32A23
B12	X0D14		4C0	8B0	16A8	32A28
B13	X0D15		4C1	8B1	16A9	32A29
B14	CLK	MAIN SYSTEM CLOCK				
B15	X0D22	1G0				
B16	GND	Ground				
B17	X0D16	XL44IN	4D0	8B2	16A10	
B18	X0D17	XL43IN	4D1	8B3	16A11	

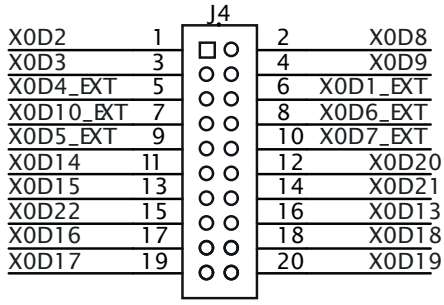

Figure 5: J4: Type-1 Slot Testpoints

2.8.2 Type-1 Slot Pinout table - Bottom side

PCIE Bottom	SIGNAL	FUNCTION					
A1	NC	No connection					
A2	+5V0	Power supply 5V voltage in/out					
A3	NC	No connection					
A4	NC	No connection					
A5	Ground	Ground					
A6	X0D08			4A2	8A6	16A6	32A26
A7	X0D09			4A3	8A7	16A7	32A27
A8	GND	Ground					
A9	X0D01_EXT	XL32OUT	1B0				
A10	X0D06_EXT			4B2	8A4	16A4	32A24
A11	X0D07_EXT			4B3	8A5	16A5	32A25
A12	X0D20			4C2	8B6	16A14	32A30
A13	X0D21			4C3	8B7	16A15	32A31
A14	Ground	Ground					
A15	X0D13		1G0				
A16	RST_N_OUT	Reset signal - xCORE-200 device					
A17	X0D18	XL42IN		4D2	8B4	16A12	
A18	X0D19	XL41IN		4D3	8B5	16A13	

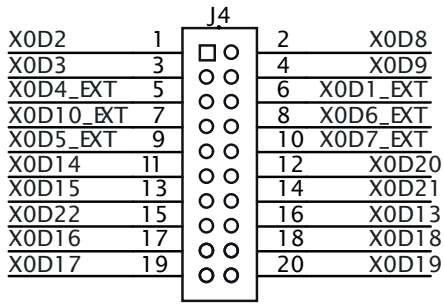

Figure 6: J4: Type-1 Slot Testpoints

2.8.3 Type-2 Slot Pinout Table - Top Side

PCIE (TOP)	SIGNAL	FUNCTION				
B1	NC	No connection				
B2	X0D0	XL32out	1B0			
B3	GND	Ground				
B4	X0D11		1D0			
B5	3.3V	+3.3V Voltage rail				
B6	X0D26	XL73out		4E0	8C0	16B0
B7	X0D27	XL74out		4E1	8C1	16B1
B8	GND	Ground				
B9	X0D28			4F0	8C2	16B2
B10	X0D34	XL71out	1K0			
B11	X0D29			4F1	8C3	16B3
B12	X0D36		1M0		8D0	16B8
B13	X0D37	XL04IN	1N0		8D1	16B9
B14	CLK	MAIN SYSTEM CLOCK				
B15	X0D24	XL70in	1I0			
B16	GND	Ground				
B17	X0D38	XL03in	1O0		8D2	16B10
B18	X0D39	XL02IN	1P0		8D3	16B11

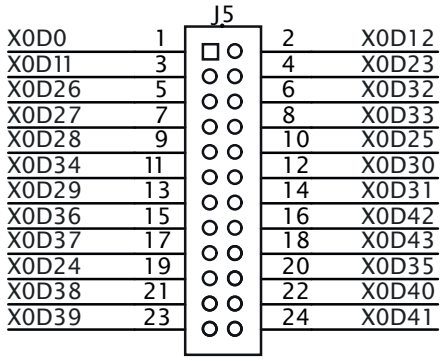

Figure 7: J5: Type-2 Slot Testpoints

2.8.4 Type-2 Slot Pinout Table - Bottom Side

PCIE Bottom	SIGNAL	FUNCTION				
A1	NC	No connection				
A2	+5V0	Power supply 5V voltage in/out				
A3	X0D11		1D0			
A4	X0D23		1H0			
A5	Ground	Ground				
A6	X0D32			4E2	8C6	16B6
A7	X0D33			4E3	8C7	16B7
A8	X0D25	XL70out	1J0			
A9	X0D30			4F2	8C4	16B4
A10	GND	Ground				
A11	X0D31			4F3	8C5	16B5
A12	X0D42	XL00out			8D6	16B14
A13	X0D43	XL01out			8D7	16B15
A14	Ground	Ground				
A15	X0D35	XL72out	1L0			
A16	RST_N_OUT	Reset signal - xCORE-200 device				
A17	X0D40	XL01IN			8D4	16B12
A18	X0D41	XL00IN			8D5	16B13

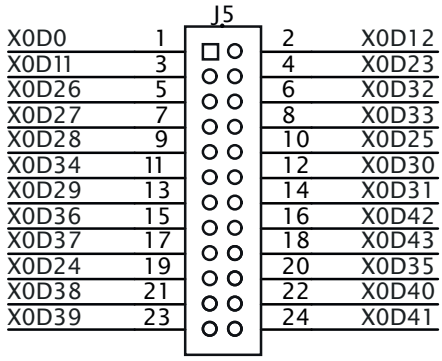

Figure 8: J5: Type-2 Slot Testpoints

2.8.5 Type-3 Slot Pinout Table - Top Side

J14 P1-2 (Marking- 'SQ') should be selected for Type-3 slot.

PCIE B (TOP)	SIGNAL	FUNCTION			
B1	*DEBUG*	XSYS DEBUG SIGNAL			
B2	*TCK*	XSYS TCK SIGNAL			
B3	*GND*	POWER SUPPLY GROUND			
B4	*TDI*	XSYS TDI SIGNAL			
B5	*3V3*	POWER SUPPLY 3.3V			
B6	X1D2	P4A0	P8A0	P16A0	P32A20
B7	X1D3	P4A1	P8A1	P16A1	P32A21
B8	*GND*	POWER SUPPLY GROUND			
B9	X1D4	P4B0	P8A2	P16A2	P32A22
B10	X1D10	P1C0			
B11	X1D5	P4B1	P8A3	P16A3	P32A23
KEY	**KEY**	**MECHANICAL KEY**			
B12	X1D14	P4C0	P8B0	P16A8	P32A28
B13	X1D15	P4C1	P8B1	P16A9	P32A29
B14	*CLK*	MAIN SYSTEM CLOCK			
B15	X1D22	P1G0			
B16	*GND*	POWER SUPPLY GROUND			
B17	X1D16	P4D0	P8B2	P16A10	
B18	X1D17	P4D1	P8B3	P16A11	

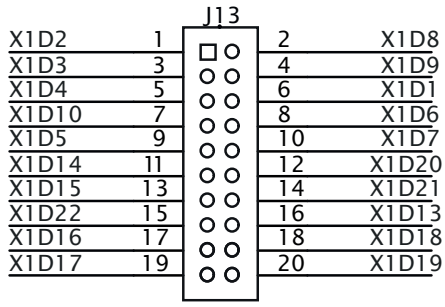

Figure 9: J13: Type-3 Slot Testpoints

2.8.6 Type-3 Slot Pinout Table - Bottom Side

PCIE A (BOT)	SIGNAL	FUNCTION
A1	*NC*	NOT CONNECTEDNAL
A2	*5V*	POWER SUPPLY 5V
A3	*TMS*	XSYS TMS SIGNAL
A4	*TDO*	XSYS TDO SIGNAL
A5	*PRSNT*	SYSTEM PRESENT SIGNAL (ACTIVE LOW)
A6	X1D8	P4A2 P8A6 P16A6 P32A26
A7	X1D9	P4A3 P8A7 P16A7 P32A27
A8	X1D1	P1B0
A9	X1D6	P4B2 P8A4 P16A4 P32A24
A10	*GND*	POWER SUPPLY GROUND
A11	X1D7	P4B3 P8A5 P16A5 P32A25
KEY	**KEY**	**MECHANICAL KEY**
A12	X1D20	P4C2 P8B6 P16A14 P32A30
A13	X1D21	P4C3 P8B7 P16A15 P32A31
A14	*GND*	POWER SUPPLY GROUND
A15	X1D13	P1F0
A16	*RST_N*	xCORE-200 RESET (ACTIVE LOW)
A17	X1D18	P4D2 P8B4 P16A12
A18	X1D19	P4D3 P8B5 P16A13

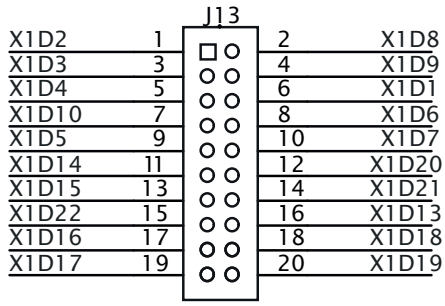

Figure 10: J13: Type-3 Slot Testpoints

2.8.7 Type-7 Slot Pinout Table - Top Side

PCIE B (TOP)	SIGNAL	FUNCTION
B1	*DEBUG*	XSYS DEBUG SIGNAL
B2	*TCK*	XSYS TCK SIGNAL
B3	*GND*	POWER SUPPLY GROUND
B4	*TDI*	XSYS TDI SIGNAL
B5	*3V3*	POWER SUPPLY 3.3V
B6	X1D57	P32A8
B7	X1D56	P32A7
B8	*GND*	POWER SUPPLY GROUND
B9	X1D55	P32A6
B10	X1D49	P32A0
B11	X1D54	P32A5
KEY	**KEY**	**MECHANICAL KEY**
B12	X1D69	P32A18
B13	X1D68	P32A17
B14	*CLK*	MAIN SYSTEM CLOCK
B15	X1D61	P32A10
B16	*GND*	POWER SUPPLY GROUND
B17	X1D67	P32A16
B18	X1D66	P32A17

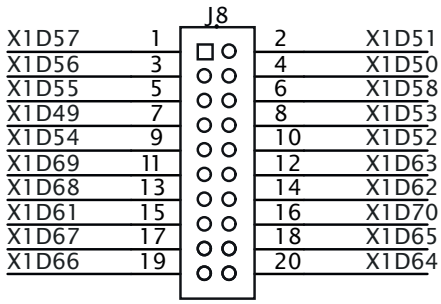

Figure 11: J8: Type-7 Slot Testpoints

2.8.8 Type-7 Slot Pinout Table - bottom Side

PCIE A (BOT)	SIGNAL	FUNCTION
A1	*NC*	NOT CONNECTED
A2	*5V*	POWER SUPPLY 5V
A3	*TMS*	XSYS TMS SIGNAL
A4	*TDO*	XSYS TDO SIGNAL
A5	*PRSNT*	SYSTEM PRESENT SIGNAL (ACTIVE LOW)
A6	X1D51	P32A2
A7	X1D50	P32A1
A8	X1D58	P32A9
A9	X1D53	P32A4
A10	*GND*	POWER SUPPLY GROUND
A11	X1D52	P32A3
KEY	**KEY**	**MECHANICAL KEY**
A12	X1D63	P32A12
A13	X1D62	P32A11
A14	*GND*	POWER SUPPLY GROUND
A15	X1D70	P32A19
A16	*RST_N*	xCORE-200 RESET (ACTIVE LOW)
A17	X1D65	P32A14
A18	X1D64	P32A13

J14 P2-3 (Marking- 'XL') should be shorted for Type-7 slot.

Slot-7 should be used for multichain muti-core board connection which includes xLINK signals.

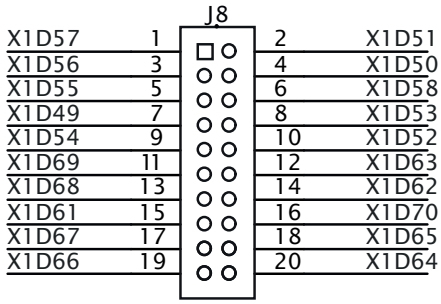

Figure 12: J8: Type-7 Slot Testpoints

2.8.9 Type-4 Slot Pinout Table - Top Side

PCIE TOP	SIGNAL	FUNCTION					
B1	NC	No connection					
B2	X1D0	XL72in	1A0				
B3	GND	Ground					
B4	X1D11	XL40in	1D0				
B5	3.3V	+3.3V Voltage rail					
B6	X1D26			4E0	8C0	16B0	
B7	X1D27			4E1	8C1	16B1	
B8	GND	Ground					
B9	X1D28			4F0	8C2	16B2	
B10	X1D34	XL02out	1K0				
B11	X1D29			4F1	8C3	16B3	
B12	X1D36	XL04out	1M0		8D0	16B8	
B13	X1D37	XL34in	1N0		8D1	16B9	
B14	CLK_OUT0	MAIN SYSTEM CLOCK					
B15	X1D24		1I0				
B16	GND	Ground					
B17	X1D38	XL33in	1O0		8D2	16B10	
B18	X1D39	XL32in	1P0		8D3	16B11	32A10

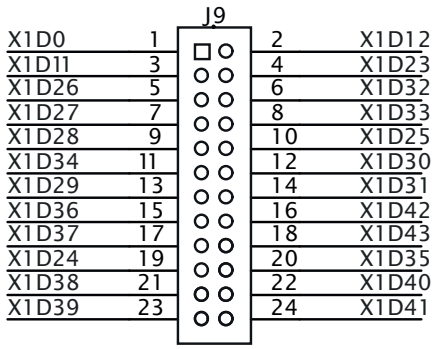

Figure 13: J9: Type-4 Slot Testpoints

2.8.10 Type-4 Slot Pinout Table - Bottom Side

PCIE Bottom	SIGNAL	FUNCTION				
A1	NC	No connection				
A2	+5V0	Power supply 5V voltage in/out				
A3	X1D12		1E0			
A4	X1D23		1H0			
A5	GND	Ground				
A6	X1D32			4E2	8C6	16B6
A7	X1D33			4E3	8C7	16B7
A8	X1D25		1J0			
A9	X1D30			4F2	8C4	16B4
A10	Ground	Ground				
A11	X1D31			4F3	8C5	16B5
A12	X1D42				8D6	16B14
A13	X1D43				8D7	16B15
A14	Ground	Ground				
A15	X1D35	XL03out	1L0			
A16	RST_N_OUT	Reset signal - xCORE-200 device				
A17	X1D40				8D4	16B12
A18	X1D41				8D5	16B13

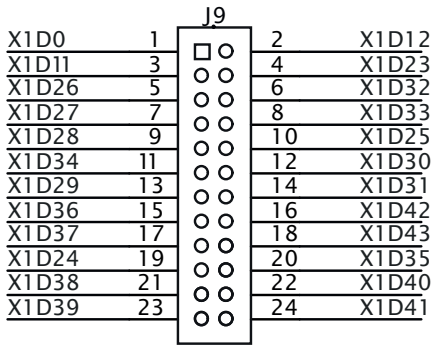

Figure 14: J9: Type-4 Slot Testpoints

2.9 System Services Slot Signals

On all Slots, TDO is always out of the sliceKIT Core Board, TDI is always in to the Core Board.

MSEL, TCK, TMS, RST_N are all inputs to the Core Board from the XSYS Connector and outputs from the Core Board on the Type-3 Slot.

DEBUG is bidirectional.

PRSNT_N is used on the Type-3 Slot to detect another Core Board is connected. This signal is used to switch the JTAG chain signals.

CLK and RST_N are output from all Slots.

2.10 xCORE-200 General Purpose sliceKIT schematics

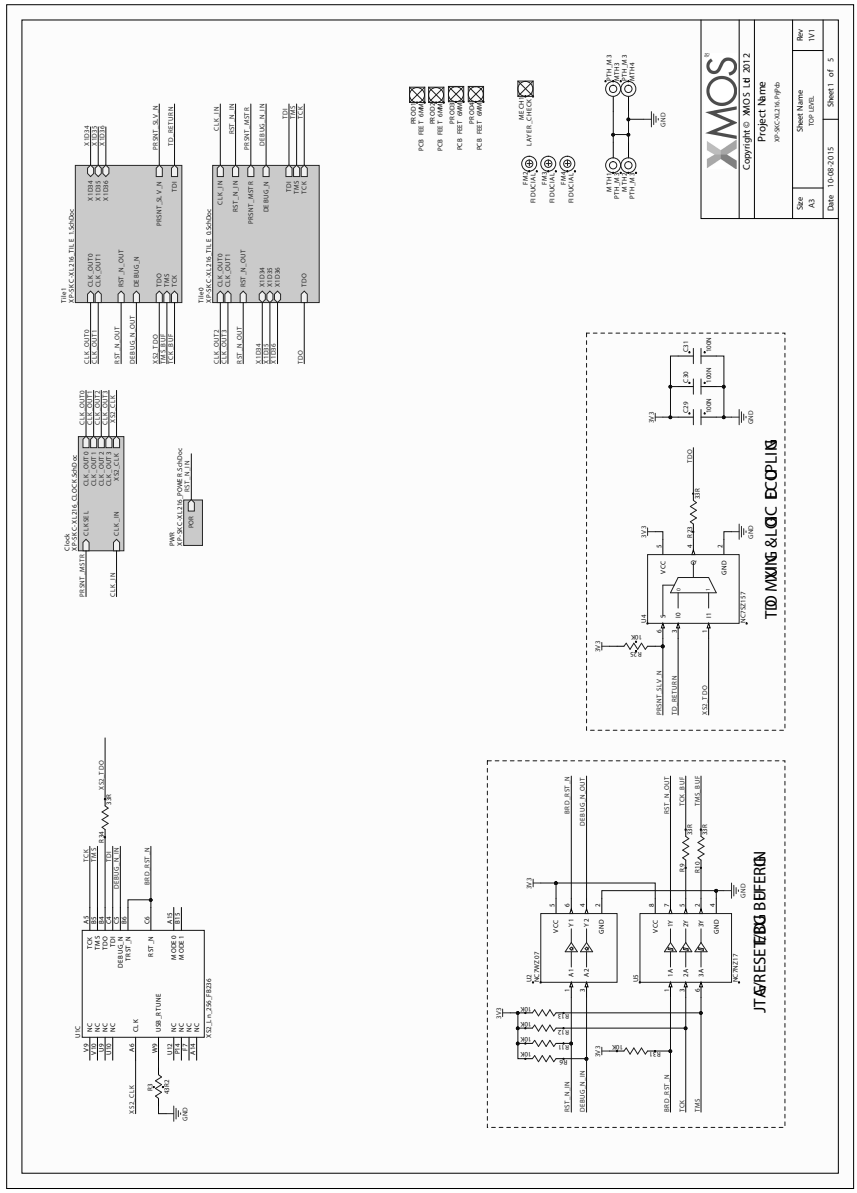

Figure 15: xCORE-200 General Purpose sliceKIT schematic (1 of 5)

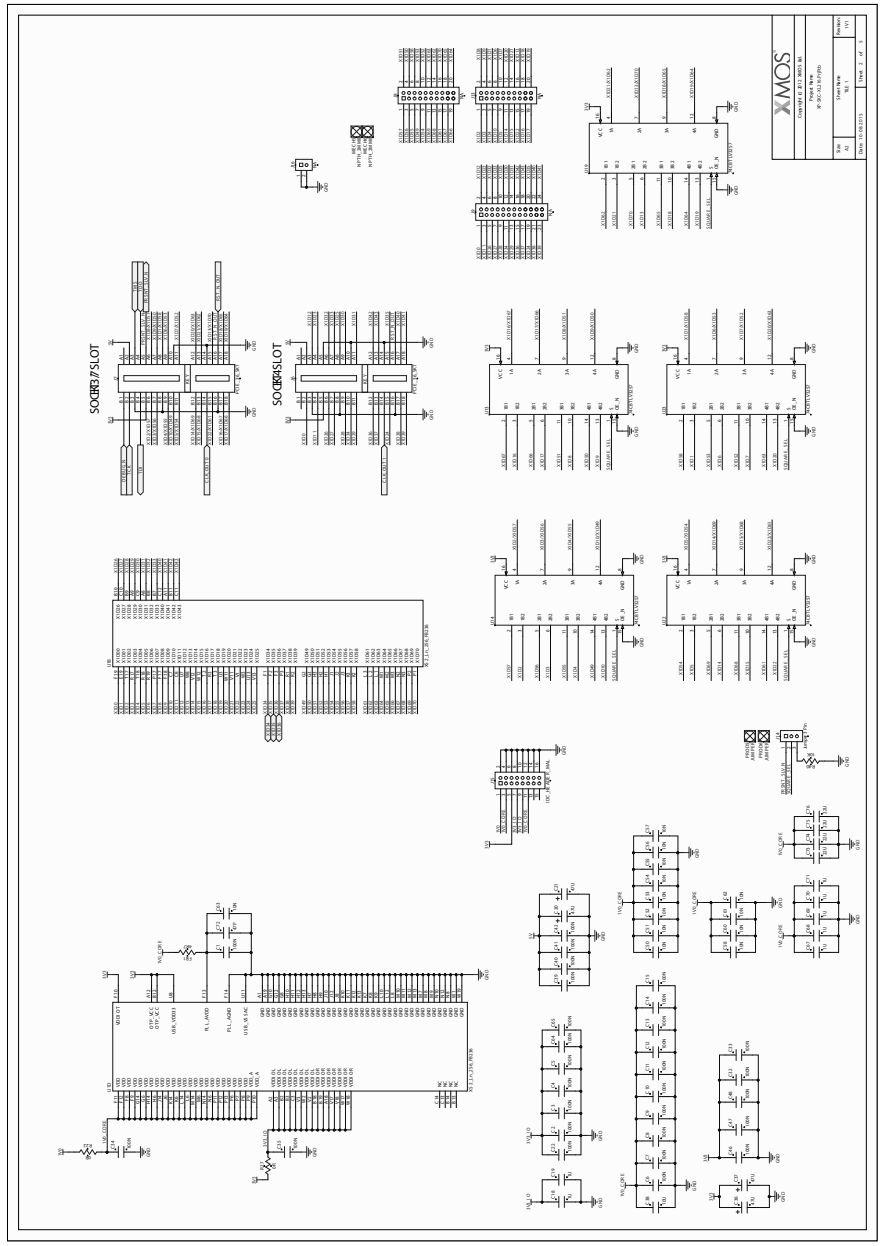

Figure 16: xCORE-200 General Purpose sliceKIT schematic (2 of 5)

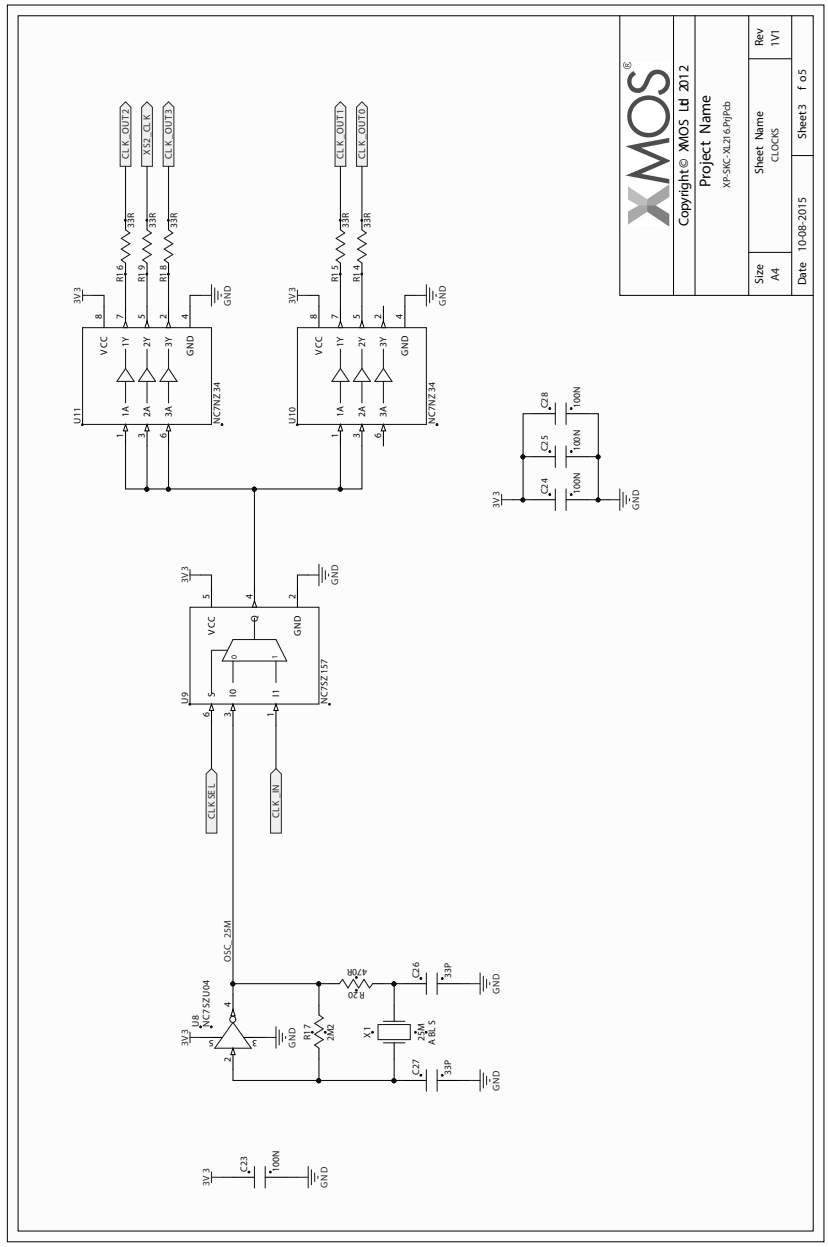

Figure 17: xCORE-200 General Purpose sliceKIT schematic (3 of 5)

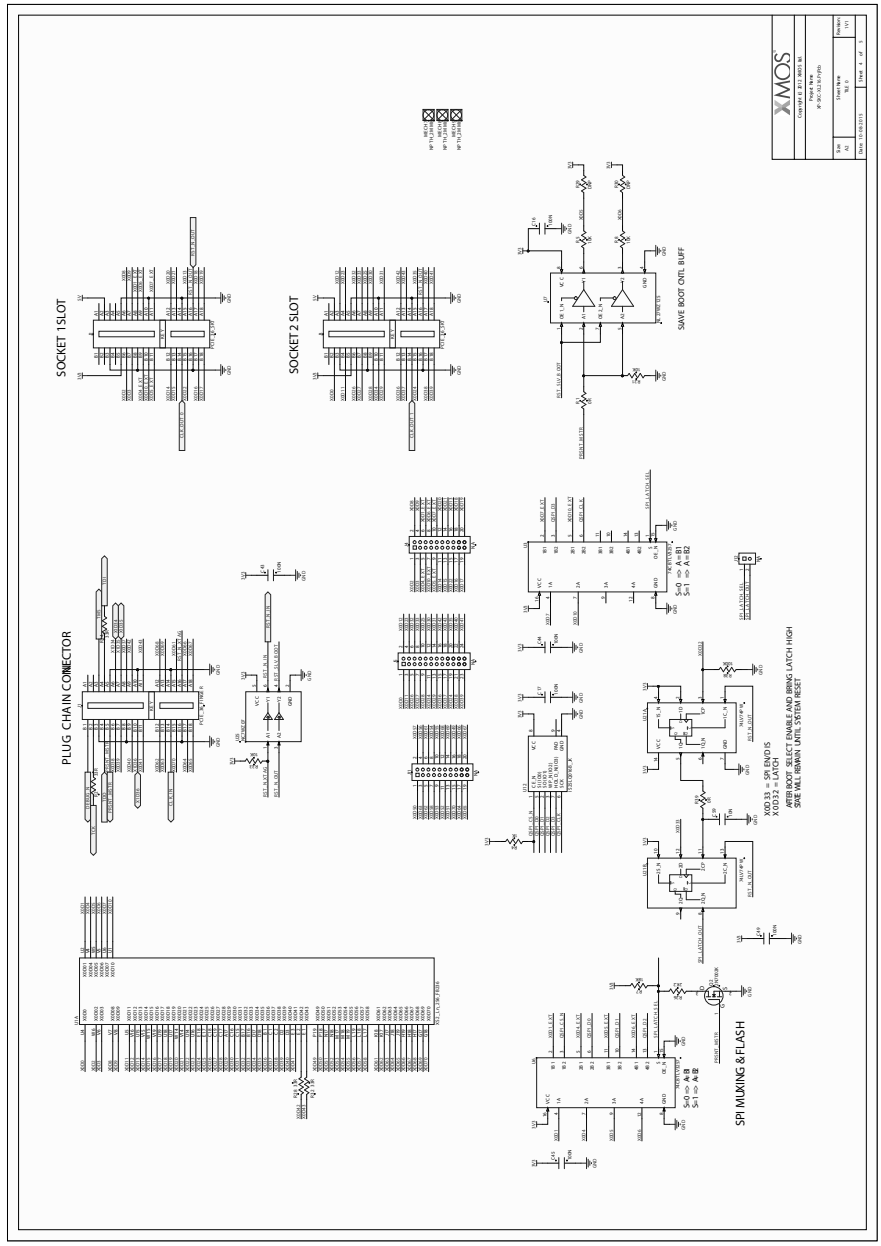

Figure 18: xCORE-200 General Purpose sliceKIT schematic (4 of 5)

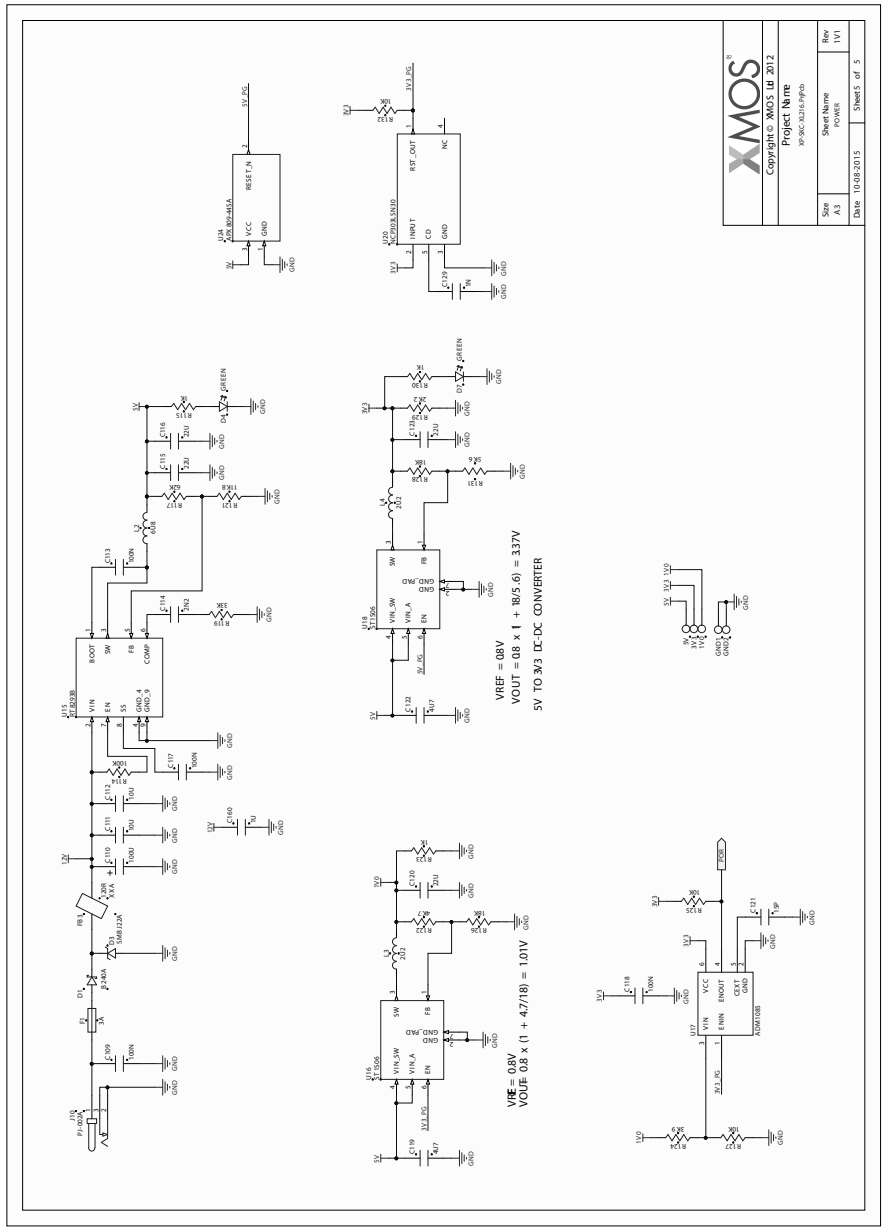

Figure 19: xCORE-200 General Purpose sliceKIT schematic (5 of 5)

3 Building multicore systems with xCORE devices

IN THIS CHAPTER

3.1 Boot sequence

3.1.1 Multiple core boards

Additional sliceKIT core boards can be connected to the xSYS slot on the first board via the Square Slot on the second board, to add extra processing capability and I/O through extra sliceCARDs. The first board is termed the `Master` and the remaining boards are `Slaves`. When there is only one board, it is the `Master`.

Slot numbering is printed on the XL Core Board silkscreen. The `Type-7` slot includes 20 xCORE I/Os (usable as GPIO or two 5-wire xCONNECT Links). The label denotes which sliceCARDs are compatible with which Core Board Slots. The sliceCARDs are also marked with one or more of these labels to identify the slot type(s) they function correctly with.

All Slots are 36 pin PCI express style connectors in either socket or edge finger (plug) types.

`Type-1` and `Type-2` Slots are pinned out from Tile 0 of the xCORE-200 XL216 device and the `Type-3/7` and `Type-4` Slots from Tile 1.

xCore-200 SliceKIT provides backward compatibility as it can be used with previous generation sliceKITs and sliceCARDs.

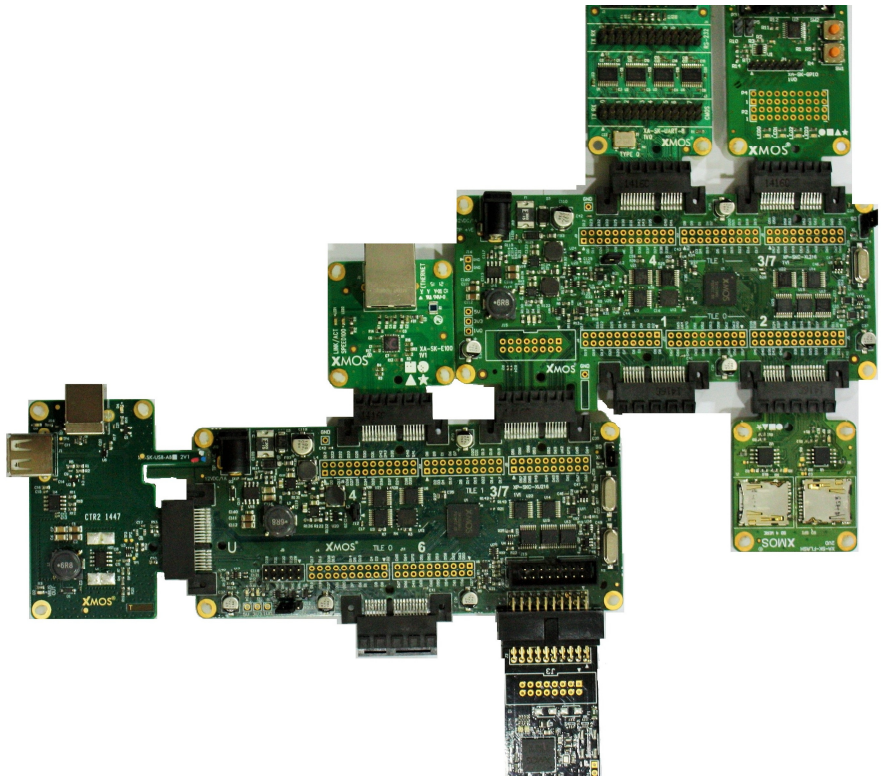

Figure 20: Example sliceKIT system diagram

4 New Designs Based on sliceKIT

IN THIS CHAPTER

There are a number of sections of the design of the sliceKIT platform that have been optimized for flexibility to cover as many use cases as possible. Therefore some consideration may be required in what to leave out or change in a custom design. Some of the important points to consider are dealt with in this section.

Some general points to consider when implementing your own design are:

- Always check the datasheet of the xCORE device. In the case where the reference design and datasheet conflict, the datasheet presides.
- XMOS datasheets contain additional hardware design requirements and guidelines that are not covered in this document, which users of XMOS hardware reference designs must ensure are followed.
- The presence of a third party device in an XMOS hardware reference design does not make any statement about its general availability. You must make your own arrangements to ensure that all components can be sourced in the required volumes.

4.1 Portmap

Due to the flexibility of the I/O on an xCORE device the location of the signals routed to the xCore-200 device can be easily optimized for your own layout.

As a general rule any 1-bit port pin can be easily swapped with any other. The only fixed 1-bit port pins are those connected to the SPI bus of the code flash device.

The location of signals on the 4-bit ports can be swapped with other signals on the same port, and the ports as a whole can be swapped, however care should be taken to ensure that all signals on the same port should be in the same direction i.e. all outputs or all inputs.

4.2 SPI Routing Control

In order to maximize the functionality of the GP SK platform all of the 1-bit ports used by the boot flash can also used by the system after boot. In order to allow for this the SPI 1-bit ports are latched to either the flash device or to the I/O.

If your design does not make use of all of the 1-bit ports then the slave select line should be left to only control the SPI interface and the rest of the SPI 1-bit ports can be reused.

4.3 Debug Interface

During the development phase of a new design it is highly recommended that the full XSYS debug interface, including the xSCOPE xCONNECT link, should be included. This allows for full programming and debug interfaces.

Once the design is stable the xSCOPE xCONNECT link can be omitted, and if space is a concern the main JTAG signals can be bought out to a custom header, or test points.

For high volume builds it is possible to omit the debug interface altogether, however this will require another method of programming the flash e.g. preprogrammed before placement.

For single device designs most of the switching and buffering devices for the JTAG chain can be omitted.