PIC16F526

PIC16F526 Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16F526

1.0 PROGRAMMING THE PIC16F526

The PIC16F526 is programmed using a serial method. The Serial mode will allow the PIC16F526 to be programmed while in the user's system. This allows for increased design flexibility. This programming specification applies to the PIC16F526 devices in all packages.

1.1 Hardware Requirements

The PIC16F526 requires one power supply for VDD (5.0V) and one for VPP (12.5V).

1.2 Program/Verify Mode

The Program/Verify mode for the PIC16F526 allows programming of user program memory, user ID locations, backup OSCCAL location and the Configuration Word.

FIGURE 1-1: PIC16F526 14-PIN PDIP, SOIC, TSSOP DIAGRAM

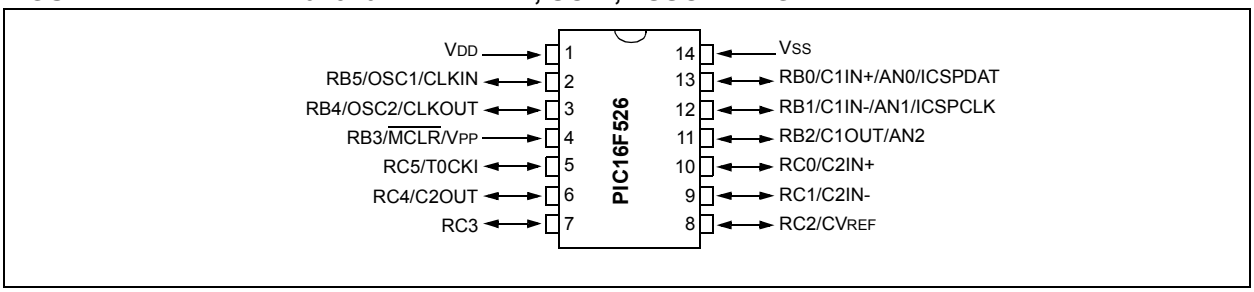


TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB1	ICSPCLK	I	Clock input – Schmitt Trigger input
RB0	ICSPDAT	I/O	Data input/output – Schmitt Trigger input
MCLR/VPP/RB3	Program/Verify mode	P(1)	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

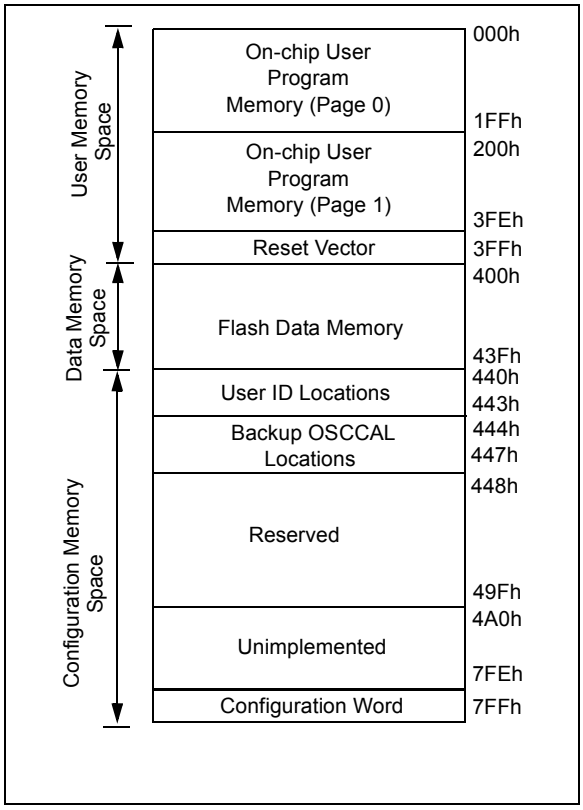
Legend: I = Input, O = Output, P = Power

Note 1: In the PIC16F526, the programming high voltage is internally generated. To activate the Program/Verify mode, high voltage of IIHH current capability (see Table 6-1) needs to be applied to the MCLR input.

2.0 MEMORY MAPPING

The Program Memory map of the PIC16F526 device is shown in Figure 2-1. In Program/Verify mode, the Program Memory extends from 0x000 to 0x7FF.

FIGURE 2-1: MEMORY MAP



2.1 User Memory

The user memory space is the on-chip user program memory. As shown in Figure 2-1, it extends from 0x000 to 0x3FF and partitions into pages, including Reset vector at address 0x3FF. Note that the PC will increment from (0x000-0x3FF) then to 0x400, (not to 0x000).

2.2 Data Memory

The data memory space is the Flash data memory block and is located at addresses PC = 400h-43Fh. All program mode commands that work on the normal Flash memory work on the Flash data memory block. This includes Bulk Erase, Load and Read Data commands.

2.3 Configuration Memory

The configuration memory space extends from 0x440 to 0x7FF. Locations from 0x448 through 0x49F are reserved. The user ID locations extend from 0x440 through 0x443. The Configuration Word is physically located at 0x7FF, and the backup OSCCAL locations extend from 0x444 through 0x447.

2.3.1 USER ID LOCATIONS

A user may store identification information (ID) in four user ID locations. The user ID locations are mapped in [0x440:0x443]. It is recommended that users use only the four Least Significant bits (LSb) of each user ID location and program the upper 8 bits as '1's. The user ID locations read out normally, even after code protection is enabled. It is recommended that user ID location is written as '1111 1111 bbbb' where 'bbbb' is user ID information.

2.3.2 CONFIGURATION WORD

The Configuration Word is physically located at 0x7FF. It is only available upon Program mode entry. Once an Increment Address command is issued, the Configuration Word is no longer accessible, regardless of the address of the program counter.

Note:	By convention, the Configuration Word is stored at the logical address location of 0xFFF within the hex file generated for the PIC16F526. This logical address location may not reflect the actual physical address for the part itself. It is the responsibility of the programming software to retrieve the Configuration Word from the logical address within the hex file and granulate the address to the proper physical location when programming.

2.3.3 BACKUP OSCCAL VALUE

The backup OSCCAL locations, 0x444-0x447, are the locations where the OSCCAL values are stored during testing of the INTOSC. This location is not erased during a standard Bulk Erase, but is erased if the PC is moved into configuration memory prior to invoking a Bulk Erase. If this value is erased, it is the user's responsibility to rewrite it back to this location for future use.

2.4 Oscillator Calibration Bits

The oscillator Calibration bits are stored at the Reset vector as the operand of a MOVLW instruction. Programming interfaces must allow users to program the Calibration bits themselves for custom trimming of the INTOSC. Capability for programming the Calibration bits when programming the entire memory array must also be maintained for backwards compatibility.

3.0 COMMANDS AND ALGORITHMS

3.1 Program/Verify Mode

The Program/Verify mode is entered by holding pins ICSPCLK and ICSPDAT low while raising VDD pin from VIL to VDD. Then raise VPP from VIL to VIHH. Once in this mode, the user program memory and configuration memory can be accessed and programmed in serial fashion. Clock and data are Schmitt Trigger input in this mode.

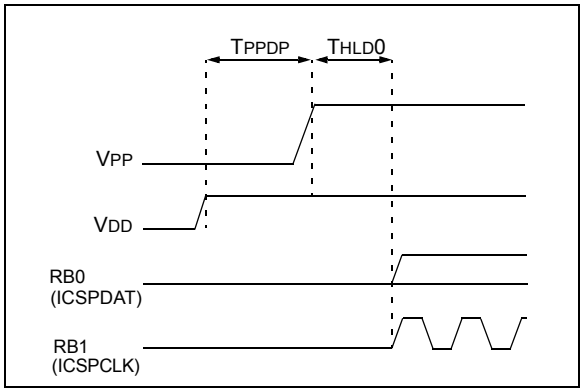
The sequence that enters the device into the Programming/Verify mode places all other logic into the Reset state (the $\overline{MCLR}$ pin was initially at VIL). This means that all I/Os are in the Reset state (high-impedance inputs).

3.1.1 PROGRAMMING

The programming sequence loads a word, programs, verifies and finally increments the PC.

Program/Verify mode entry will set the address to 0x7FF. The Increment Address command will increment the PC. The available commands are shown in Table 3-1.

FIGURE 3-1: ENTERING HIGH VOLTAGE PROGRAM/ VERIFY MODE



3.1.2 SERIAL PROGRAM/VERIFY OPERATION

The RB1 pin is used as a clock input pin, and the RB0 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB1) is cycled 6 times. Each command bit is latched on the falling edge of the clock with the Least Significant bit (LSb) of the command being input first. The data on pin RB0 is required to have a minimum setup and hold time of 100 ns with respect to the falling edge of the clock. Commands that have data associated with them (Read and Load) are specified to have a minimum delay of 1 µs between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a Start bit and the last cycle being a Stop bit. Data is also input and output LSb first, with data input being latched on the falling edge of the clock and data output being driven on the rising edge of the clock. Therefore, during a Read operation the LSb will be transmitted onto pin RB0 on the rising edge of the second cycle, and during a Load operation the LSb will be latched on the falling edge of the second cycle. A minimum 1 µs delay is also specified between consecutive commands; except the “End Programming” command which requires a 100 µs delay. Because this is a 12-bit core, the two MSbs of the data word are ignored. The commands that are available are described in Table 3-1.

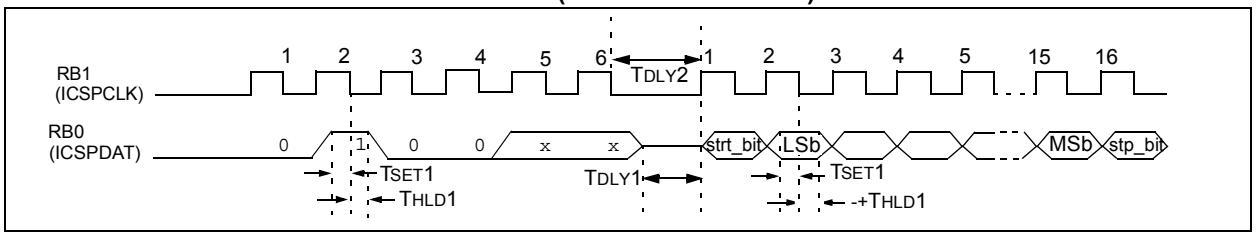
TABLE 3-1: COMMAND MAPPING LOAD DATA

Command	Mapping (MSb ... LSb)	Hex Value	Data
Load Data	X X 0 0 1 0	2	start_bit, data (14), stop_bit
Read Data	X X 0 1 0 0	4	start_bit, data (14), stop_bit
Increment Address	X X 0 1 1 0	6	
Begin Programming	X X 1 0 0 0	8	
End Programming	X X 1 1 1 0	E	
Bulk Erase Program Memory	X X 1 0 0 1	9	

3.1.2.1 Load Data

After receiving this command, the device will clock in 14 bits as a “data word” when 16 cycles are applied, as described previously. Because this is a 12-bit core, the two MSbs of the data word are ignored. A timing diagram for the Load Data command is shown in Figure 3-2.

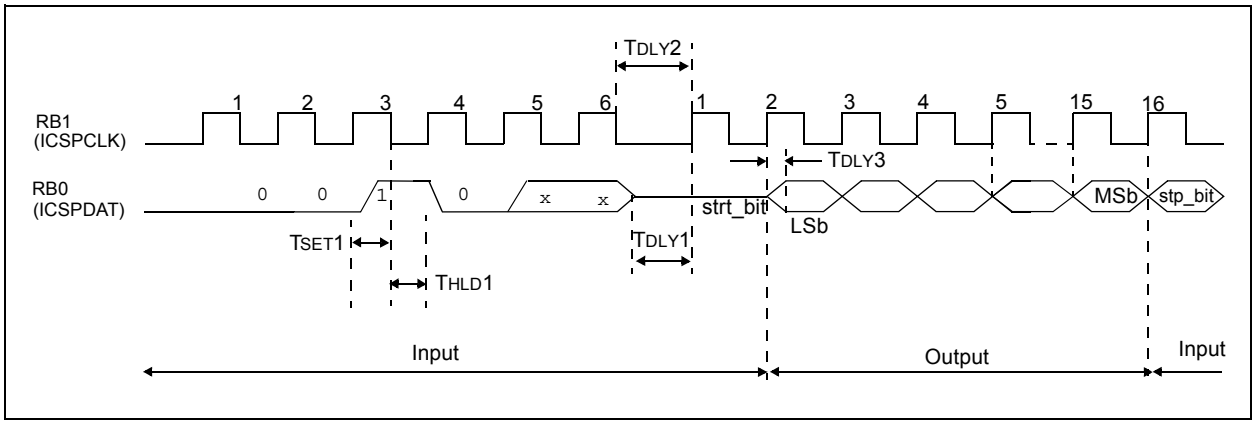
FIGURE 3-2: LOAD DATA COMMAND (PROGRAM/VERIFY)



3.1.2.2 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB0 pin will go into Output mode on the second rising clock edge and it will revert back to Input mode (high-impedance) after the 16th rising edge. Because this is a 12-bit core, the two MSbs will read as ‘1’. A timing diagram of this command is shown in Figure 3-3.

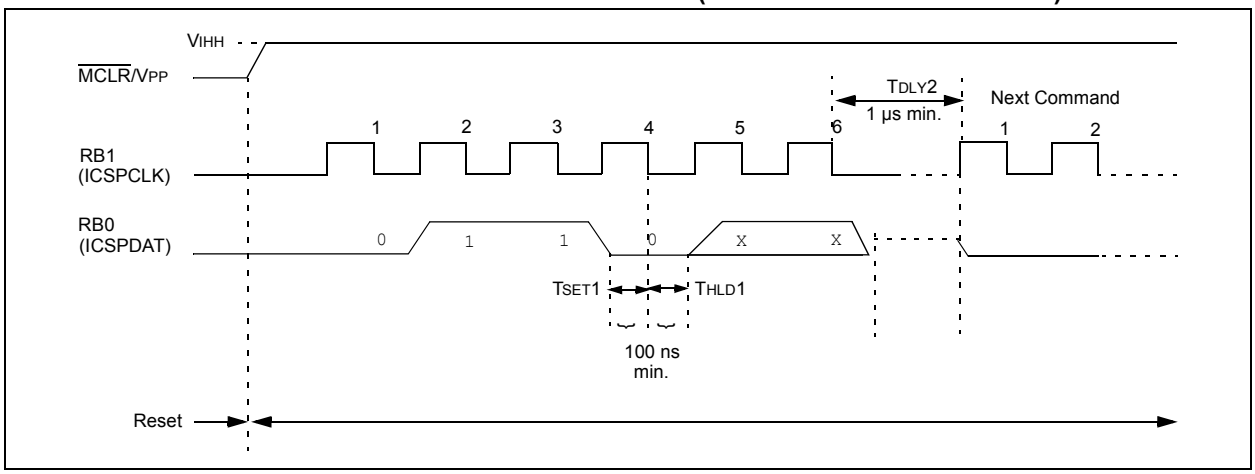
FIGURE 3-3: READ DATA FROM PROGRAM MEMORY COMMAND



3.1.2.3 Increment Address

The PC is incremented when this command is received.

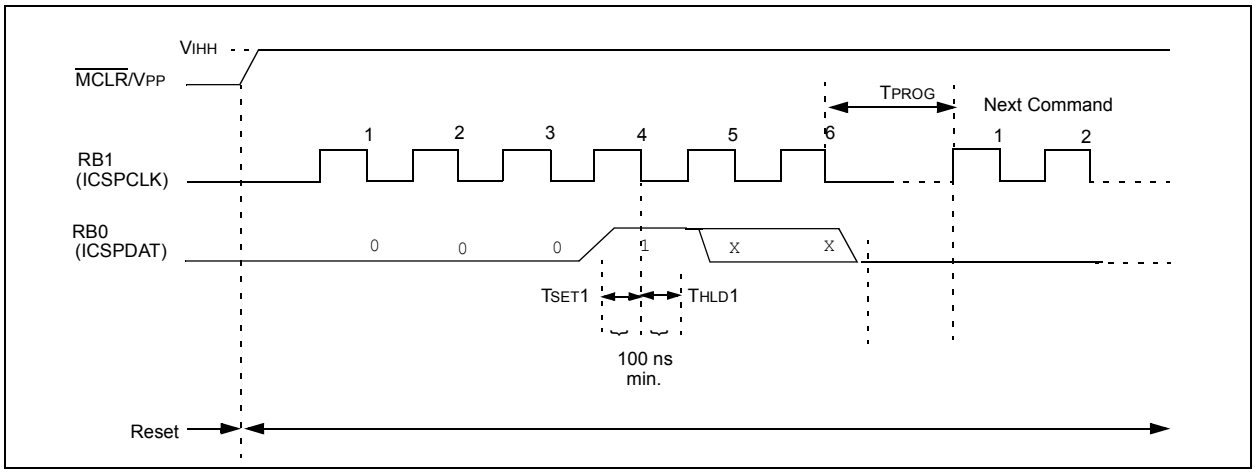
FIGURE 3-4: INCREMENT ADDRESS COMMAND (SERIAL PROGRAM/VERIFY)



3.1.2.4 Begin Programming

A Load command (Load Data) must be given before every Begin Programming command. Programming of the appropriate memory (User Program Memory, Flash Data Memory or Test Program Memory) will begin after this command is received and decoded.

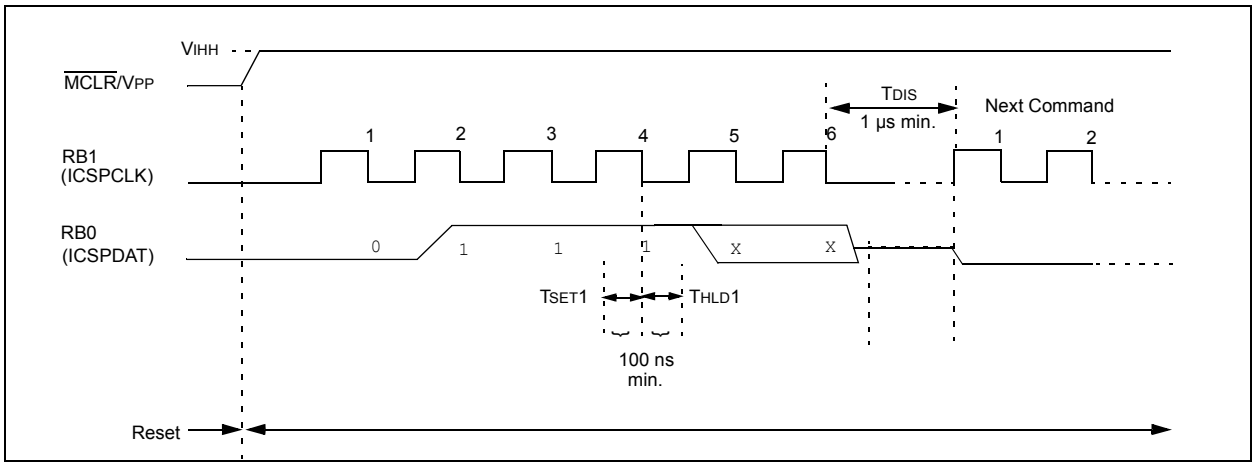
FIGURE 3-5: BEGIN PROGRAMMING COMMAND



3.1.2.5 End Programming

After receiving this command, the chip stops programming the memory (User Program Memory, Flash Data Memory or Test Program Memory) it was programming at the time.

FIGURE 3-6: END PROGRAMMING COMMAND



3.1.2.6 Bulk Erase Program Memory

After this command is performed, the specific section of Program Memory and Configuration Word is erased. See Table 3-2 for details.

Note 1:	A fully erased part will read '1's in every Program Memory location.
2:	The oscillator Calibration bits are erased if a Bulk Erase is invoked. They must be read and saved prior to erasing the device and restored during the programming operation. Oscillator Calibration bits are stored at the Reset vector as the operand of a MOVLW instruction.

FIGURE 3-7: BULK ERASE PROGRAM MEMORY COMMAND

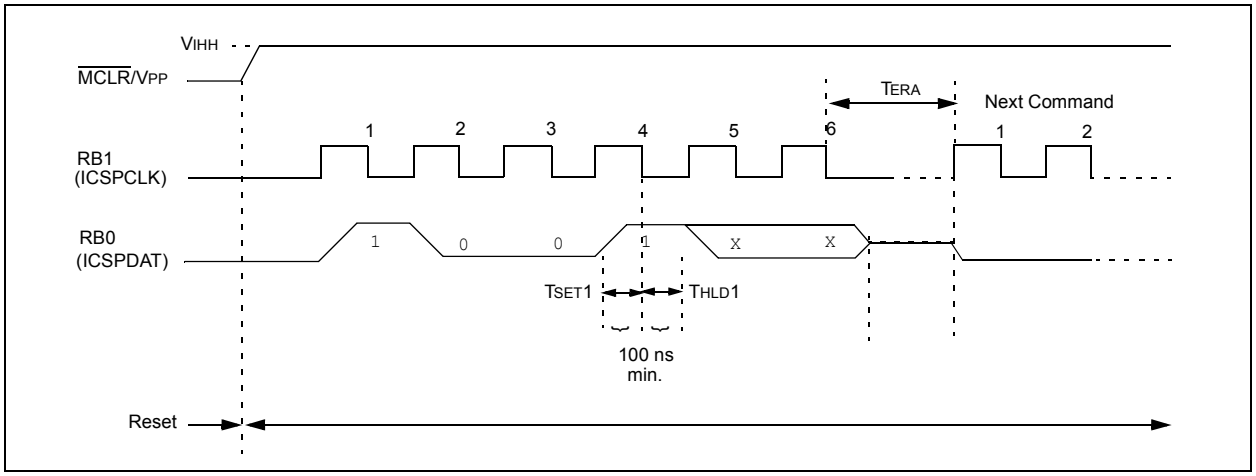


TABLE 3-2: BULK ERASE MEMORY PORTIONS

PC	Config. Word (Fuses)	User Program Memory Erased	Flash Data Memory Erased	User ID Memory Erased
Configuration Word (Fuses)	Yes	Yes	$\overline{\text{CPDF}}$ = 0 – Yes $\overline{\text{CPDF}}$ = 1 – No	No
000h-3FFh (User Memory)	Yes	Yes	$\overline{\text{CPDF}}$ = 0 – Yes $\overline{\text{CPDF}}$ = 1 – No	No
400h-43Fh (Data Memory)	No	No	$\overline{\text{CPDF}}$ = 0 – No $\overline{\text{CPDF}}$ = 1 – Yes	No
440h-447h (Configuration Memory)	No	No	No	Yes

Note: Yes = Erase
No = Unchanged

FIGURE 3-8: READING AND TEMPORARY SAVING OF THE OSCCAL CALIBRATION BITS

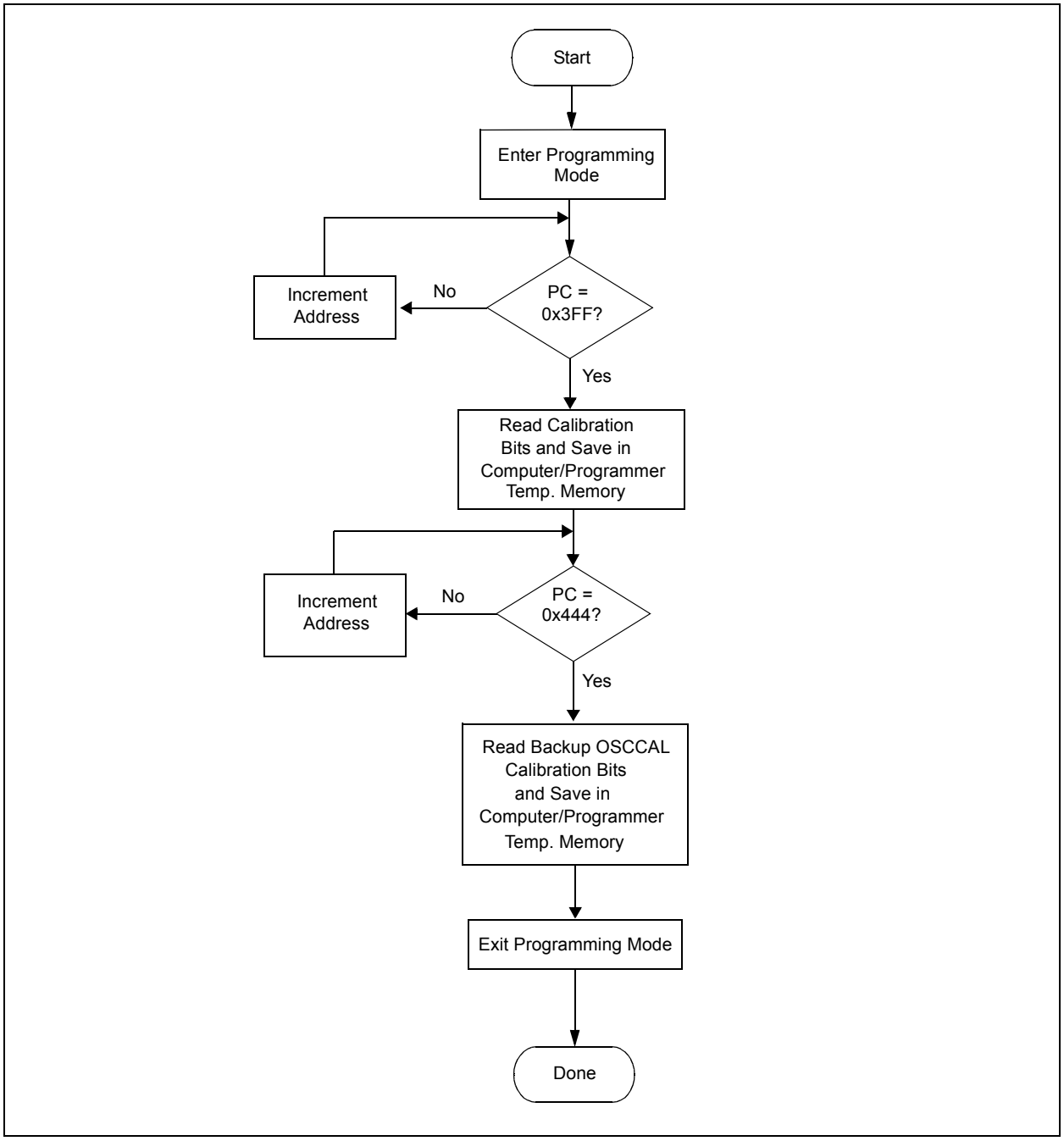


FIGURE 3-9: RESTORING/PROGRAMMING THE OSCCAL CALIBRATION BITS

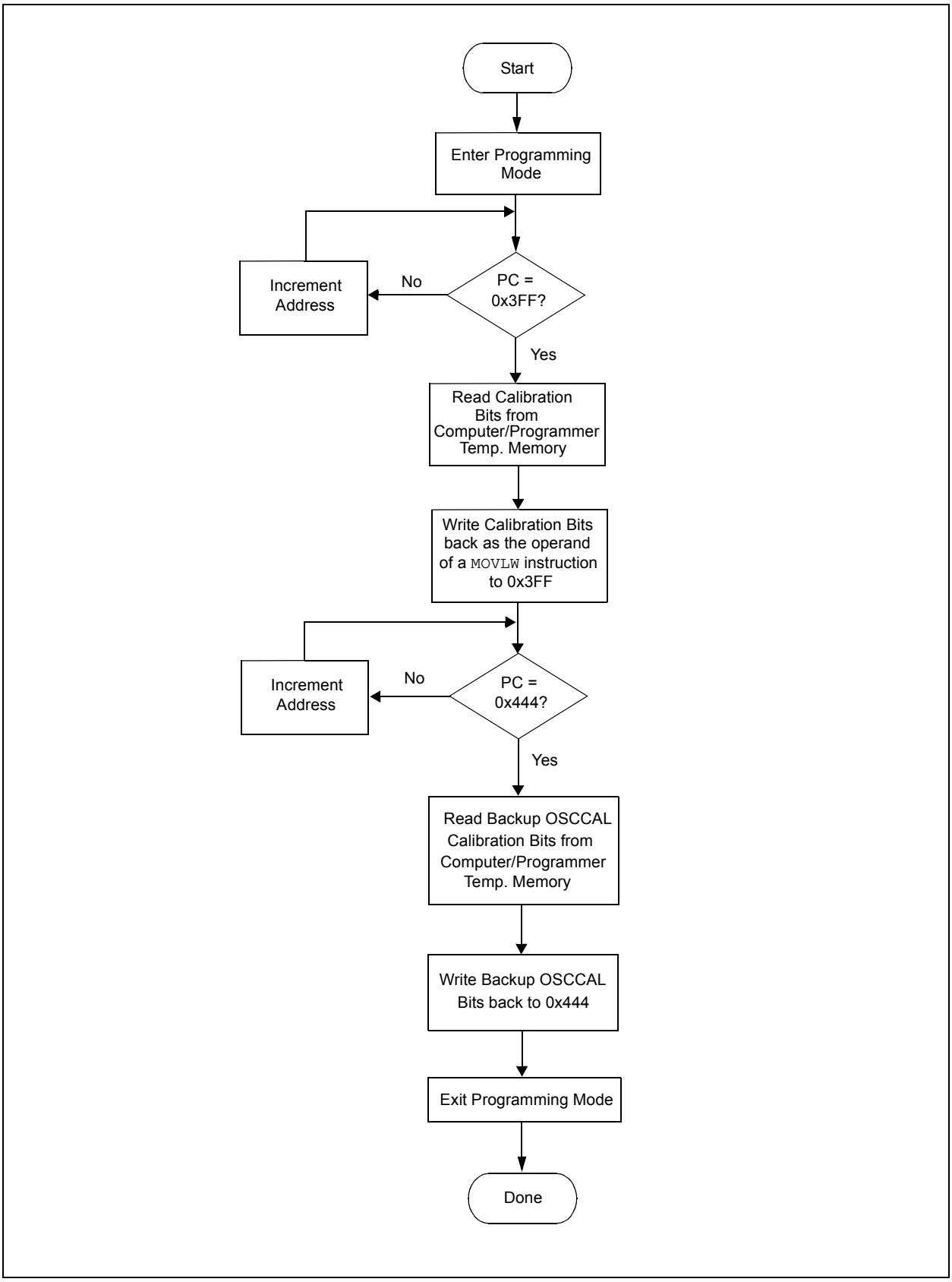


FIGURE 3-10: PROGRAM FLOWCHART – USER MEMORY

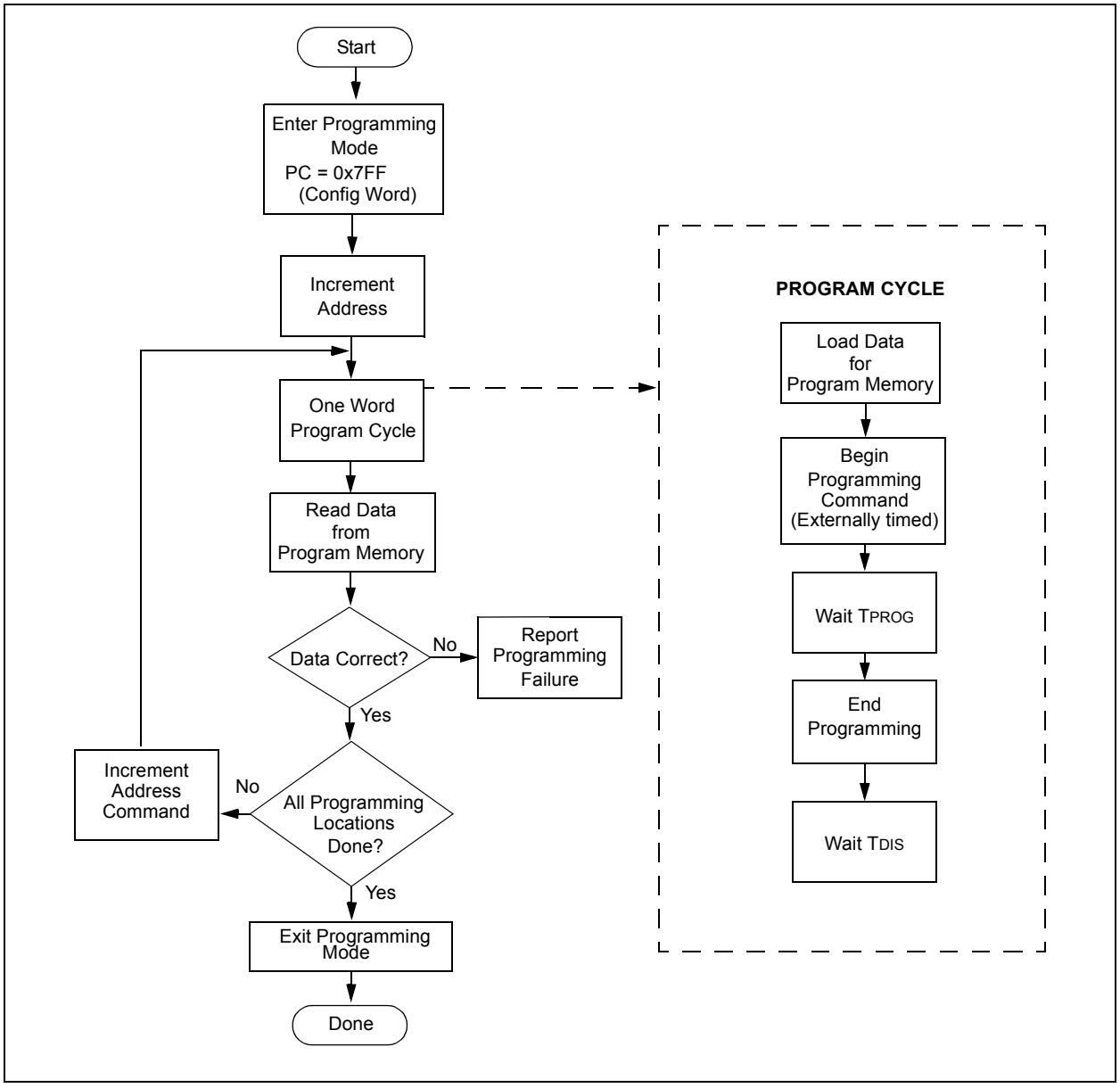


FIGURE 3-11: PROGRAM FLOWCHART – FLASH DATA MEMORY

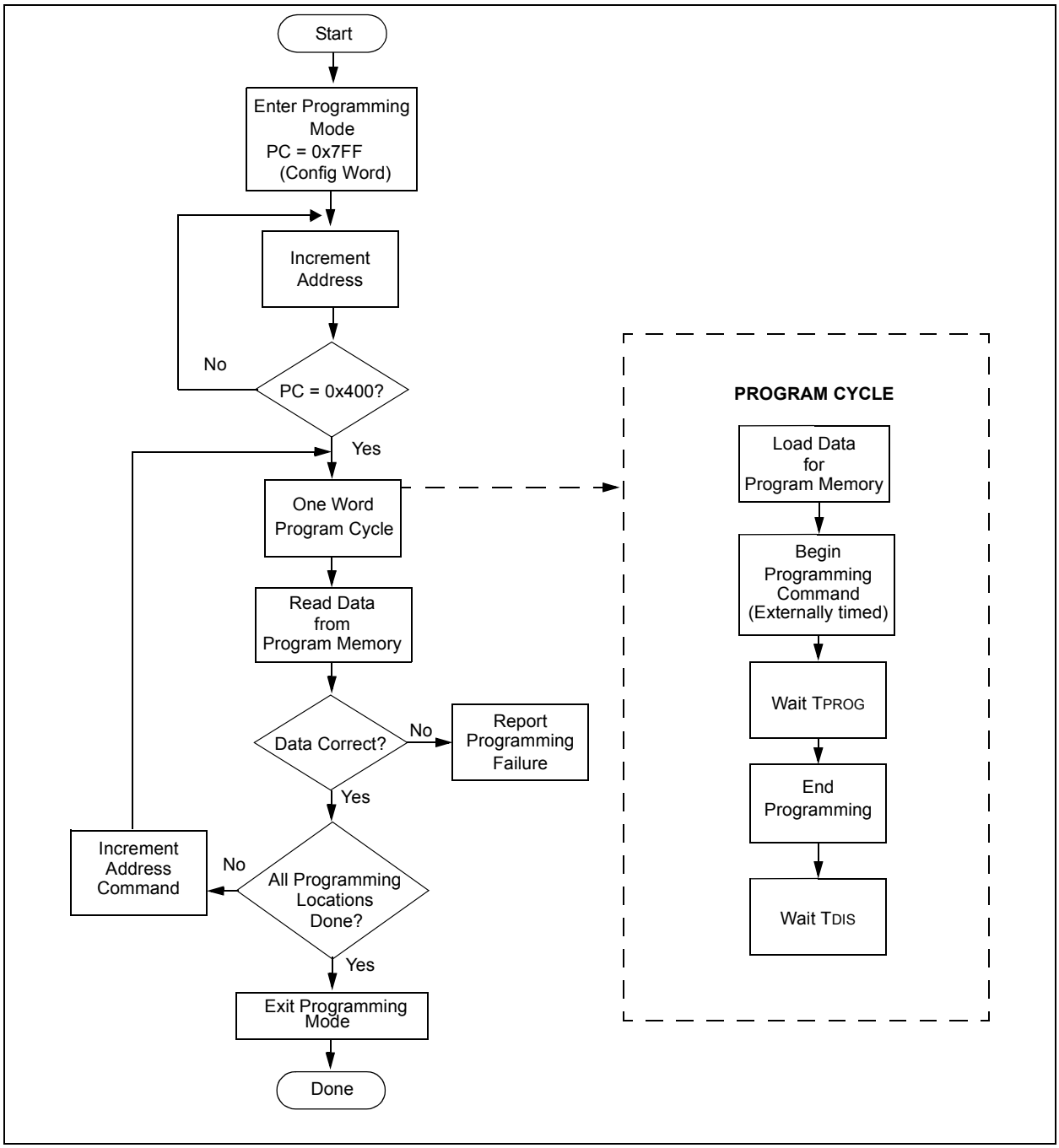


FIGURE 3-12: PROGRAM FLOWCHART – CONFIGURATION MEMORY

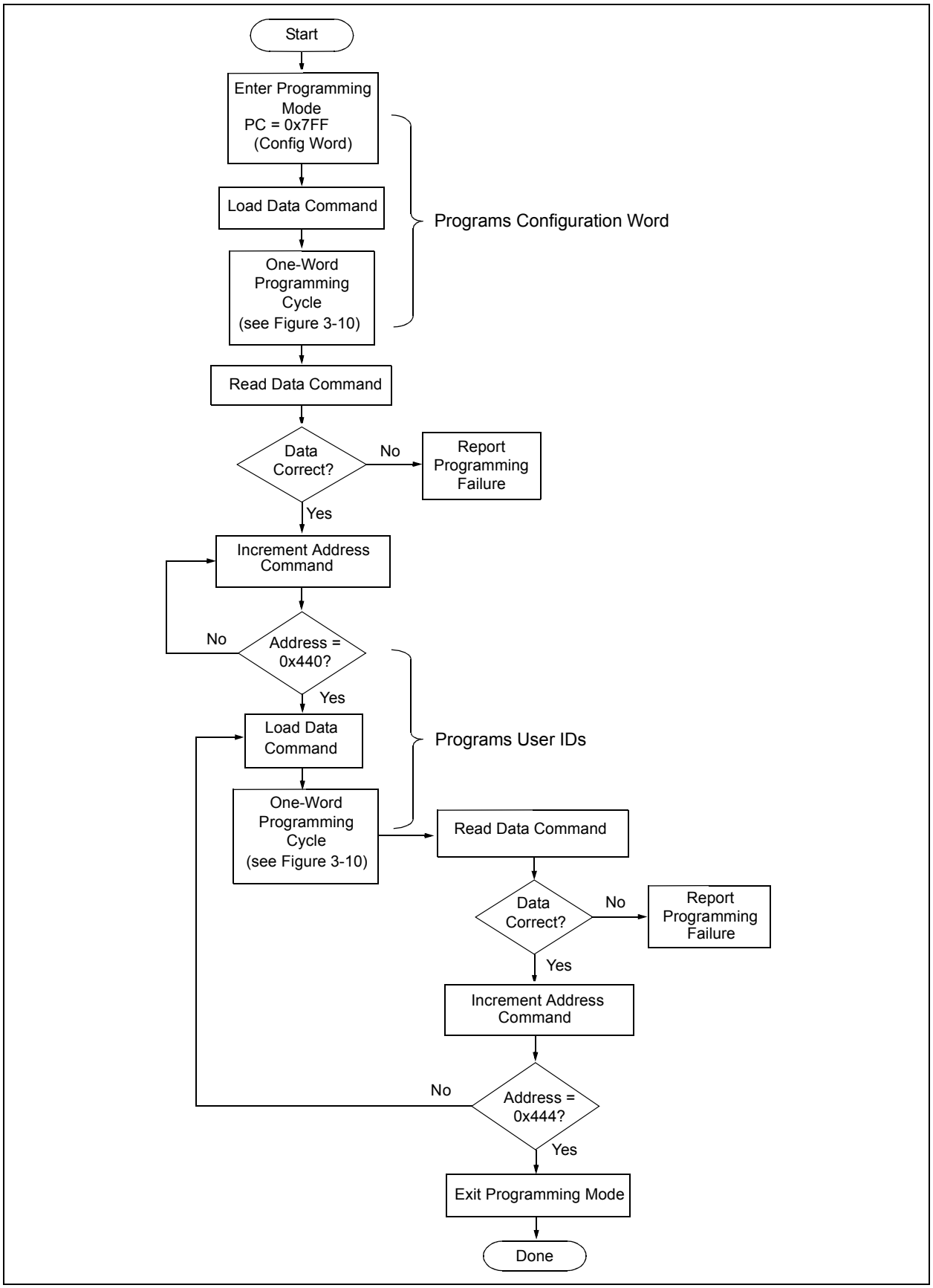
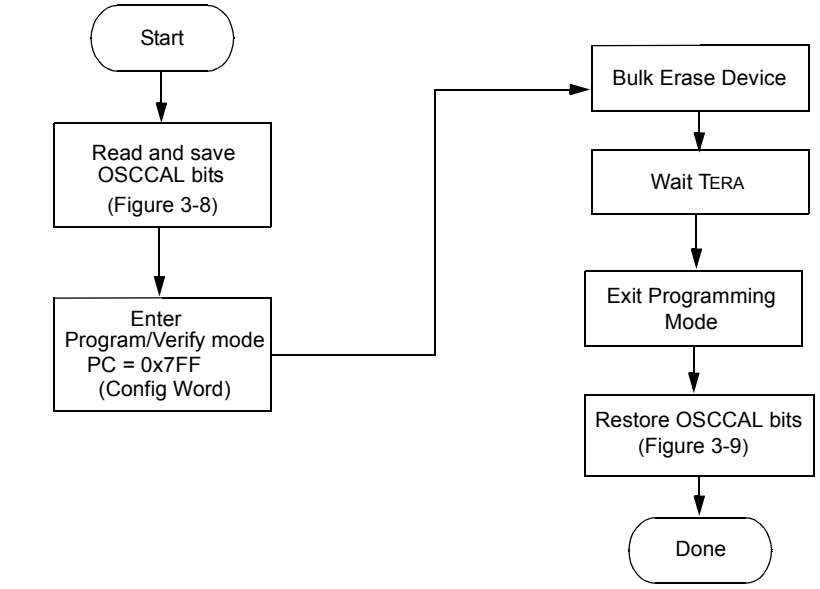
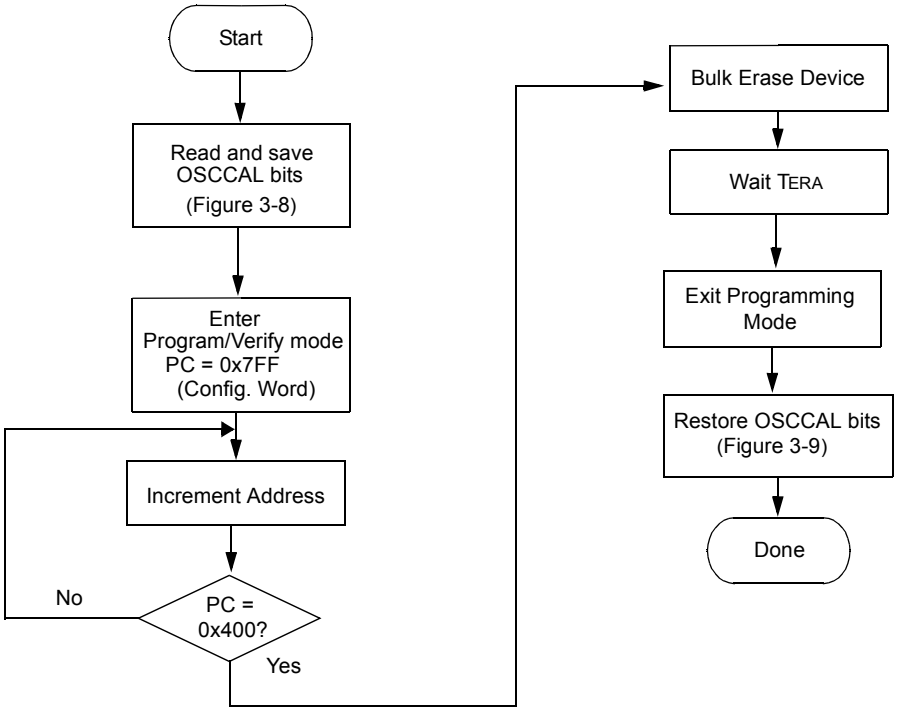


FIGURE 3-13: PROGRAM FLOWCHART – ERASE PROGRAM MEMORY, CONFIGURATION WORD



Note: Flash Data Memory block will also be erased if $\overline{CPDF}$ = 0 (see Table 3-2 for more information).

FIGURE 3-14: PROGRAM FLOWCHART – ERASE FLASH DATA MEMORY



Note 1: This operation requires that $\overline{CPDF}$ = 1.

FIGURE 3-15: PROGRAM FLOWCHART – ERASE USER ID

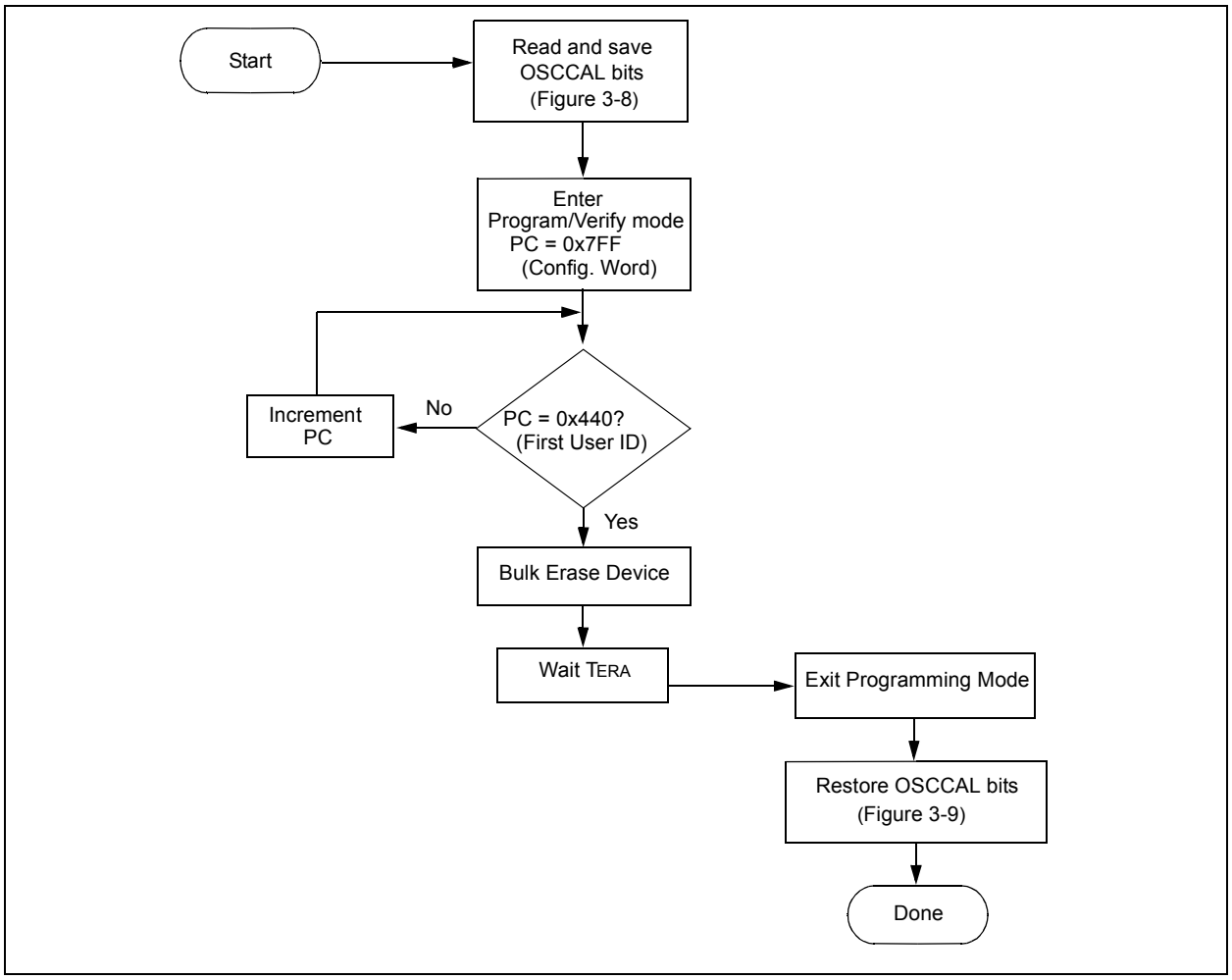


FIGURE 3-16: PROGRAM FLOWCHART – HIGH-LEVEL FULL DEVICE PROGRAM

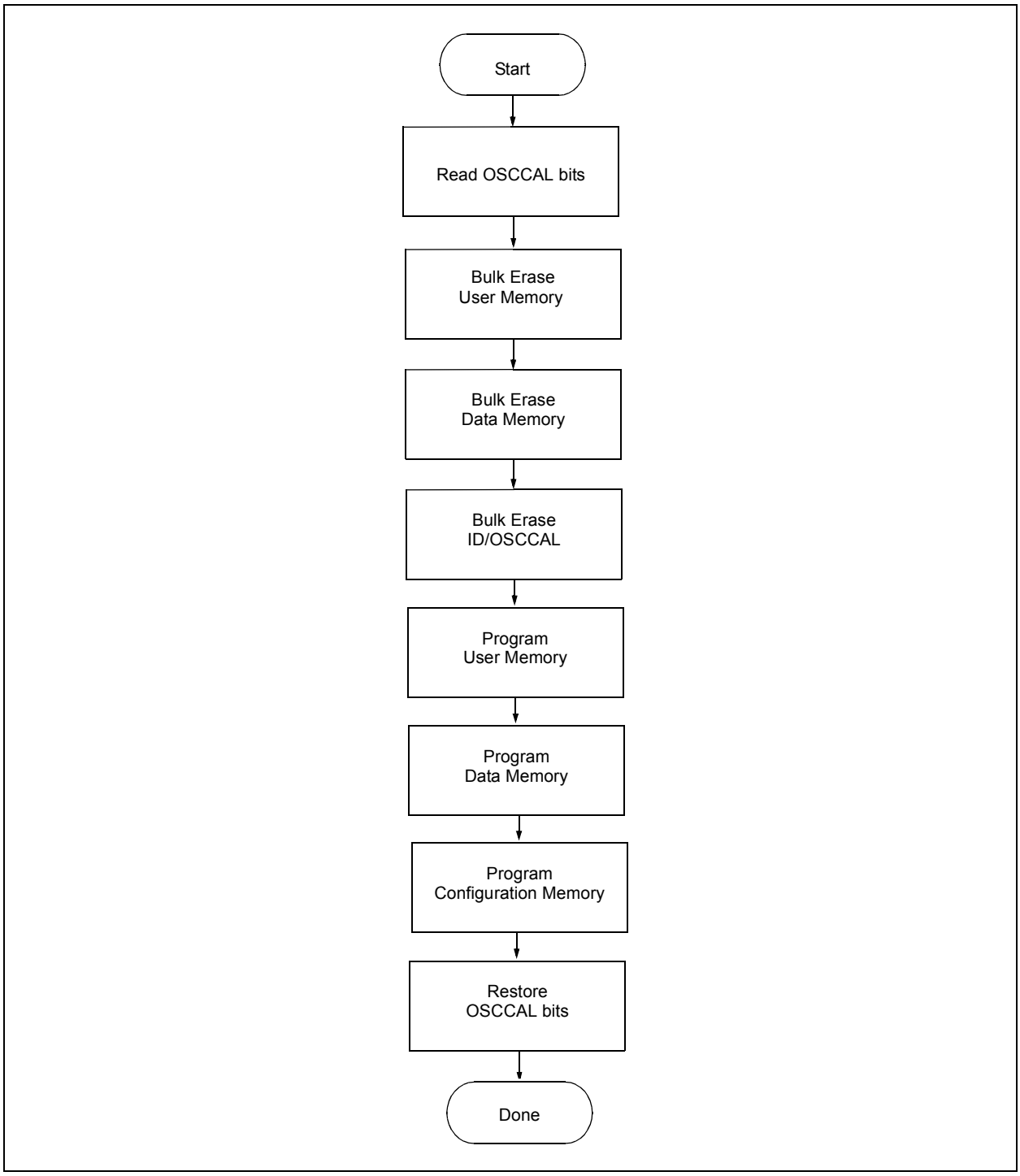
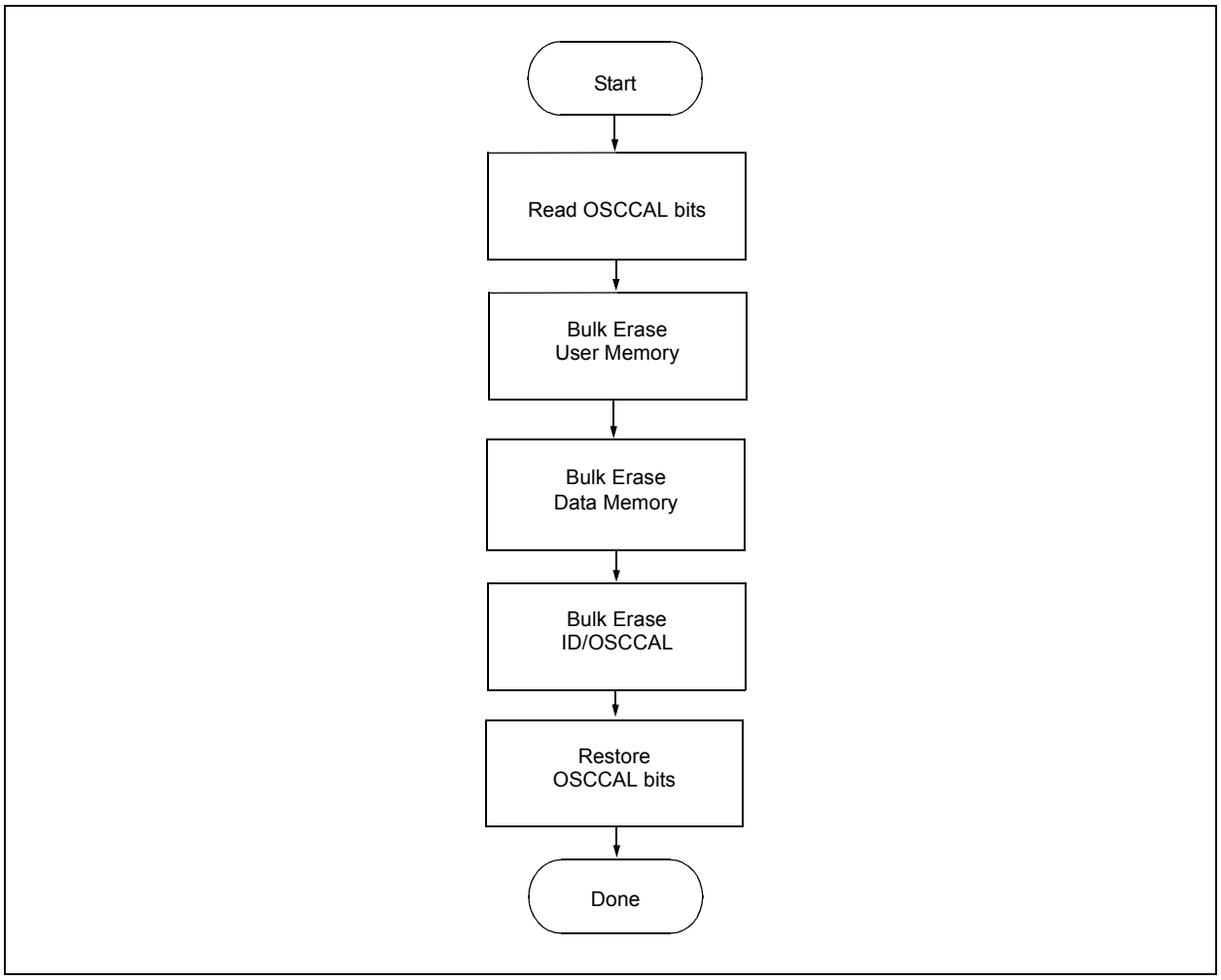


FIGURE 3-17: PROGRAM FLOWCHART – HIGH-LEVEL FULL DEVICE ERASE



4.0 CONFIGURATION WORD

The implemented Configuration bits can be programmed at their default values, or they are not programmed.

See REGISTER 4-1 below for details.

REGISTER 4-1: CONFIGURATION WORD

—	—	—	—	$\overline{\text{CPDF}}$	IOSCFS	MCLRE	$\overline{\text{CP}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 11											bit 0

bit 11-8: **Unimplemented:** Read as '1'

bit 7: **$\overline{\text{CPDF}}$:** Code Protection bit – Flash Data Memory
- 1 = Code protection off
- 0 = Code protection on

bit 6: **IOSCFS:** Internal Oscillator Frequency Select bit
- 1 = 8 MHz INTOSC speed
- 0 = 4 MHz INTOSC speed

bit 5: **MCLRE:** Master Clear Enable bit
- 1 = RB3/$\overline{\text{MCLR}}$ pin functions as $\overline{\text{MCLR}}$
- 0 = RB3/$\overline{\text{MCLR}}$ pin functions as RB3, $\overline{\text{MCLR}}$ tied internally to V_{DD}

bit 4: **$\overline{\text{CP}}$:** Code Protection bit – User Program Memory
- 1 = Code protection off
- 0 = Code protection on

bit 3: **WDTE:** Watchdog Timer Enable bit
- 1 = WDT enabled
- 0 = WDT disabled

bit 2-0: **FOSC2:FOSC0:** Oscillator Selection bits
- 000 = LP oscillator and 18 ms DRT
- 001 = XT oscillator and 18 ms DRT
- 010 = HS oscillator and 18 ms DRT
- 011 = EC oscillator with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT(1)
- 100 =INTRC with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT(1)
- 101 = INTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1 ms DRT(1)
- 110 = EXTRC with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT(1)
- 111 = EXTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1 ms DRT(1)

Note 1: It is the responsibility of the application designer to ensure the use of the 1 ms DRT will result in acceptable operation. Refer to Electrical Specifications for V_{DD} rise time and stability requirements for this mode of operation.

5.0 CODE PROTECTION

For the PIC16F526, once code protection is enabled, all Program Memory locations 0x40-0x3FE, read all '0's. Program Memory locations 0x000-0x03F and 0x3FF are always unprotected. The user ID locations, backup OSCCAL location and the Configuration Word read out in an unprotected fashion. It is possible to program the user ID locations, backup OSCCAL location and the Configuration Word after code-protect is enabled.

The code protection of the Flash data memory is dependant on the $\overline{\text{CPDF}}$ bit. If the $\overline{\text{CPDF}}$ bit is set, only the Flash data memory block is code protected. See Table 3-2 for erase conditions involving the $\overline{\text{CPDF}}$ bit.

5.1 Disabling Code Protection

It is recommended that the following procedure be performed before any other programming is attempted. It is also possible to turn code protection off using this procedure. However, ***all data within the program memory will be erased when this procedure is executed, and thus, the security of the code is not compromised.*** See Table 3-2 for more information on Flash data memory.

To disable code-protect:

a) Enter Program mode
b) Execute Bulk Erase Program Memory command (001001).
c) Wait TERA

Note: To allow portability of code, the programmer is required to read the Configuration Word and user ID locations from the hex file when loading the hex file. If Configuration Word information was not present in the hex file, then a simple warning message may be issued. Similarly, while saving a hex file, Configuration Word and user ID information must be included. An option to not include this information may be provided.

Microchip Technology Incorporated feels strongly that this feature is important for the benefit of the end customer.

5.2 Checksum Computation

5.2.1 CHECKSUM

Checksum is calculated by reading the contents of the PIC16F526 memory locations and adding up the opcodes up to the maximum user addressable location. Any Carry bits exceeding 16 bits are neglected. Finally, the Configuration Word (appropriately masked) is added to the checksum. The checksum computation for the PIC16F526 is shown in Table 5-1.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The Configuration Word, appropriately masked
- Masked user ID locations (when applicable)

The Least Significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each PIC16F526.

Note: The checksum calculation differs depending on the code-protect setting. The Configuration Word and user ID locations can always be read regardless of the code-protect settings.

TABLE 5-1: CHECKSUM COMPUTATIONS(1)

Device	Code-Protect	Checksum*	Blank Value	0x723 at 0 and Max. Address
PIC16F526	OFF	SUM[0x000:0x3FE] + CFGW & 0x0FF	0xED00	0xDB48
	ON	SUM[0x00:0x3F] + CFGW & 0x0FF + SUM_ID	0xEDAF	0xD31B

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = User ID locations masked by 0xF then made into a 16-bit value with ID0 as the Most Significant nibble. For example, ID0 = 0x1, ID1 = 0x2, ID2 = 0x3, ID3 = 0x4, then SUM_ID = 0x1234.
*Checksum = [Sum of all the individual expressions] MODULO [0xFFFF]
+ = Addition
& = Bitwise AND

Note 1: Checksum shown assumes that SUM_ID contains the unprotected checksum.

6.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 6-1: AC/DC TIMING REQUIREMENTS

AC TARGETS						
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
General						
VIHH	VPP High voltage on $\overline{MCLR}$ for Program/Verify mode entry	12.5	—	13.5	V	
VIHL	Voltage on $\overline{MCLR}$ to be in Normal mode	VSS	—	VDD + 1.0	V	
TVHHR	$\overline{MCLR}$ rise time (VSS to VHH) for Test mode entry	—	—	1.0	μs	
VIH1	Clock (RB1) and Data (RB0) input high-level	0.85*VDD	—	—	V	
VIL1	Clock (RB1) and Data (RB0) input low-level	—	—	0.15*VDD	V	
VDDOK	Minimum VDD to perform Bulk Erase	4.5	4.0	5.5	V	
VPROG	High voltage on $\overline{MCLR}$ for programming	12.5	13.0	13.5	V	
IDDPROG	IDD level for programming operations, program memory	—	—	1.8	mA	
IDDERA	IDD level for Bulk Erase operations, program memory	—	—	1.8	mA	
IPP	$\overline{MCLR}$ pin current during Program/Verify mode	—	—	0.4	mA	
TPROG	Programming time	1000	—	2000	μs	
TPPDP	Hold time after VPP↑	5	—	—	μs	
THLD0	ISPCLK, ISPDATA hold time after $\overline{MCLR}$↑ (Program/Verify mode selection pattern setup time)	5	—	—	μs	
Serial Program/Verify						
TSET1	Data in setup time before clock↓	100	—	—	ns	
THLD1	Data in hold time after clock↓	100	—	—	ns	
TDLY1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	μs	
TDLY2	Delay between clock↓ to clock↑ of next command or data	1.0	—	—	μs	
TDLY3	Clock↑ to data out valid (during Read Data)	80	—	—	ns	
TERA	Bulk Erase Time	4	—	10	ms	Total time to perform both stages of Bulk Erase and accept the next command.
TDIS	High Voltage Discharge Time	100	—	—	μs	Time to discharge high voltage.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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ISO/TS 16949:2002

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