# **DRF100**

15V, 8A, 30MHz



## MOSFET Driver Hvbrid

The DRF100 is a High-Speed Power MOSFET driver with a unique anti-ring function. It is intended to drive the gate of a power MOSFET with  $\geq$ 3nF gate capacitance to 15V at frequencies up to 30MHz. It can produce output currents  $\geq$ 8A RMS, while dissipating 60W. The Driver output can be configured as Inverting or Non-Inverting.

#### **FEATURES**

- Switching Frequency: DC TO 30MHz
- Low Pulse Width Distortion
- Single Power Supply
- 1V CMOS Schmitt Trigger Input 1V Hysteresis
- Inverting Non-Inverting Select
- RoHS Compliant

#### **Driver Absolute Maximum Ratings**

Symbol	Parameter	Min	Тур	Max	Unit
V <sub>DD</sub>	Supply Voltage			15	V
IN	Input Single Voltages			7 to +5.5	v
I <sub>орк</sub>	Output Current Peak			8	А
T <sub>JMAX</sub>	Operating Temperature			175	°C

• Output Capable of ≥ 8A RMS

• Power Dissipation Capability 60W

#### **Driver Specifications**

Symbol	Parameter	Min	Тур	Max	Unit
$V_{DD}$	Supply Voltage	10		15	v
IN	Input Voltage	3		5.5	
IN <sub>(R)</sub>	Input Voltage Rising Edge		3		
IN <sub>(F)</sub>	Input Voltage Falling Edge		3		ns
I <sub>DDQ</sub>	Quiescent Current		2		mA
I <sub>o</sub>	Output Current		8		A
C <sub>oss</sub>	Output Capacitance		2500		
C <sub>iss</sub>	Input Capacitance		3		pF
R <sub>IN</sub>	Input Parallel Resistance		1		MΩ
V <sub>T(ON)</sub>	Input, Low to High Out (See truth table)	2.0		2.8	
V <sub>T(OFF)</sub>	Input, High to Low Out (See truth table)	1.0	1	1.4	V
T <sub>DLY</sub>	Time Delay (throughput)	25		38	ns
t <sub>r</sub>	Rise Time	1.5	2.5	3.0	
t <sub>r</sub>	Fall Time	1.5	2.5	3.0	ns
T <sub>D</sub>	Prop. Delay	1	35		1



### **TYPICAL APPLICATIONS**

- MOSFET Drivers
- Switch Mode Power Amplifiers
- Digital Output Amplifiers
- Pulse Generators
- Laser Diode Drivers
- Ultrasound Transducer Drivers
- Acoustic Optical Modulators

#### **Output Characteristics**

DRF100

Symbol	Parameter	Min	Тур	Max	Unit	
C <sub>out</sub>	Output Capacitance		2500		pF	
R <sub>out</sub>	Output Resistance		1		Ω	
L <sub>out</sub>	Output Inductance	2	3	4	nH	
F <sub>MAX</sub>	Operating Frequency CL=3nF + 50Ω			30		
F <sub>MAX</sub>	Operating Frequency RL=50Ω			50	50 MHz	

#### **Thermal Characteristics**

Symbol	Parameter	Min	Тур	Max	Unit	
R <sub>θJC</sub>	Thermal Resistance Junction to Case		1.5	°C/W		
R <sub>ØJHS</sub>	Thermal Resistance Junction to Heat Sink		2.53	C/vv		
T <sub>JSTG</sub>	Storage Temperature		-55 to150		°C	
P <sub>DHS</sub>	Maximum Power Dissipation @ T <sub>SINK</sub> = 25°C		60	60 W		
P <sub>DC</sub>	Total Power Dissipation @ $T_{C} = 25^{\circ}C$		100		vv	

Microsemi reserves the right to change, without notice, the specifications and information contained herein.





The Simplified DRF100 Circuit Diagram is illustrated above. By including the driver high speed by-pass capacitor (C Internal), the contribution to the internal parasitic loop inductance of the driver output is greatly reduced. This low parasitic approach, coupled with the Schmitt trigger input (pin 4), Kelvin signal ground (pin 5) and the Anti-Ring Function, provide improved stability and control. The IN pin (4) is applied to a Schmitt Trigger. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. The P channel and N channel power drivers provide the high current to the OUTPUT (pin 9.)

The Function (FN, pin 3) is the invert or non-invert select Pin, it is Internally held high, Normally Non-inverting.

Truth Table *Referenced to SG				
FN (pin 3)*	IN (pin 4)*	Function	OUTPUT	
HIGH	HIGH	Non-Invert	HIGH	
HIGH	LOW	Non-Invert	LOW	
LOW	HIGH	Inverting	LOW	
LOW	LOW	Inverting	HIGH	





The Test Circuit illustrated above was used to evaluate the DRF100 (available as an evaluation Board DRF100 / EVALSW.) The input control signal is applied to the DRF100 via IN(4) and SG(5) pins using RG188. This provides excellent noise immunity and control of the signal ground currents.

The +V<sub>DD</sub> inputs (2,6) are by-passed (C1, C2, C4-C9), this is in addition to the internal by-passing mentioned previously. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load.

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Microsemi's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 6,939,743 7,352,045 5,283,201 5,801,417 5,648,283 7,196,634 6,664,594 7,157,886 6,939,743 7,342,262 and foreign patents. US and Foreign patents pending. All Rights Reserved.

Pin Assignments			
Pin 1	Ground		
Pin 2	+Vdd		
Pin 3	FN		
Pin 4	IN		
Pin 5	SG		
Pin 6	+Vdd		
Pin 7	Ground		
Pin 8	Source		
Pin 9	Drain		
Pin 10	Source		



All dimensions are  $\pm .005$ 

Figure 3, DRF100 Mechanical Outline