INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT563

Octal D-type transparent latch; 3-state; inverting

Product specification
File under Integrated Circuits, IC06

December 1990





Octal D-type transparent latch; 3-state; inverting

74HC/HCT563

FEATURES

- 3-state inverting outputs for bus oriented applications
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessor
- Common 3-state output enable input
- · Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT563 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT563 are octal D-type transparent latches featuring separate D-type inputs for each latch and inverting 3-state outputs for bus oriented applications.

A latch enable (LE) input and an output enable (OE) input are common to all latches.

The "563" is functionally identical to the "573", but has inverted outputs.

The "563" consists of eight D-type transparent latches with 3-state inverting outputs. The LE and $\overline{\text{OE}}$ are

common to all latches.

When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the 8 latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}C$; $t_r = t_f = 6 \, \text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT	
	PARAMETER		НС	нст	UNII
t _{PHL} / t _{PLH}	propagation delay D_n , LE to \overline{Q}_n	C _L = 15 pF; V _{CC} = 5 V	14	16	ns
Cı	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz

f_o = output frequency in MHz

 $\sum (C_1 \times V_{CC}^2 \times f_0) = \text{sum of outputs}$

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC} for HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

ORDERING INFORMATION

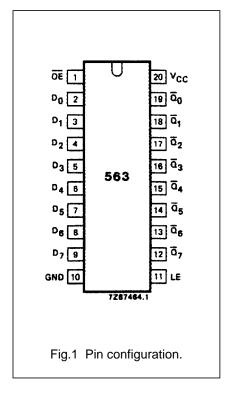
See "74HC/HCT/HCU/HCMOS Logic Package Information".

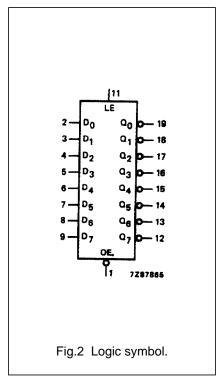
Octal D-type transparent latch; 3-state; inverting

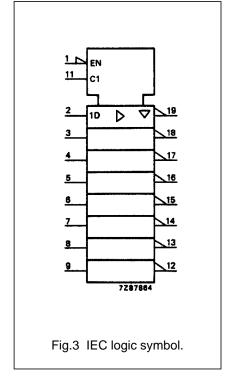
74HC/HCT563

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D ₀ to D ₇	data inputs
11	LE	latch enable input (active HIGH)
1	ŌĒ	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	\overline{Q}_0 to \overline{Q}_7	3-state latch outputs
20	V _{CC}	positive supply voltage

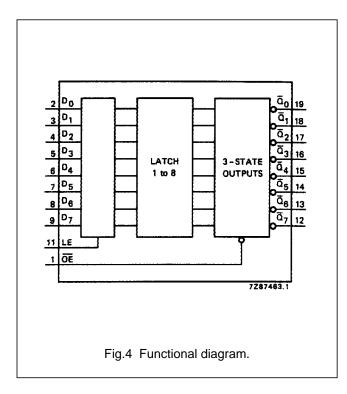






Octal D-type transparent latch; 3-state; inverting

74HC/HCT563

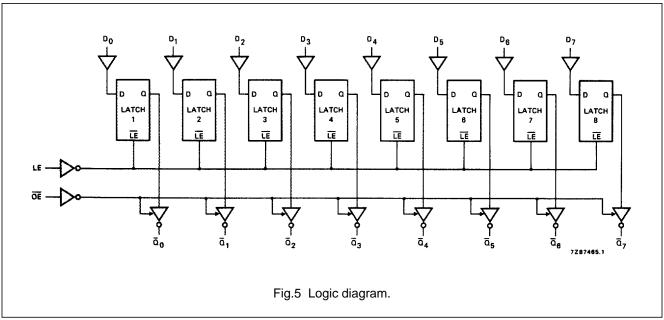


FUNCTION TABLE

OPERATING MODES	IN	IPUT	S	INTER- NAL	OUT- PUTS		
WIODES	ŌΕ	LE	Dn	LATCHES	$\overline{\mathbf{Q}}_0$ to $\overline{\mathbf{Q}}_7$		
enable and read register	L	H	L	L	H		
	L	H	H	H	L		
latch and read register	L	L	l	L	H		
	L	L	h	H	L		
latch register and disable outputs	H	L	l	L	Z		
	H	L	h	H	Z		

Notes

- 1. H = HIGH voltage level
 - h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
 - L = LOW voltage level
 - I = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
 - Z = high impedance OFF-state



Octal D-type transparent latch; 3-state; inverting

74HC/HCT563

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
SYMBOL			74HC								
		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(*)	
t _{PHL} / t _{PLH}			47	145		180		220	ns	2.0	Fig.6
	D _n to Q _n		17 14	29 25		36 31		44 38		4.5 6.0	
t _{PHL} / t _{PLH}	propagation delay		47	145		180		220	ns	2.0	Fig.7
	LE to $\overline{\mathbb{Q}}_{n}$		17 14	29 25		36 31		44 38		4.5 6.0	
t _{PZH} / t _{PZL}	3-state output enable time		47 17	150 30		190 38		225 45	ns	2.0 4.5	Fig.8
	OE to Q _n		14	26		33		38		6.0	
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} to \overline{Q}_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t _W	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t _{su}	set-up time D _n to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.9
t _h	hold time D _n to LE	4 4 4	-6 -2 -2		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig.9

Octal D-type transparent latch; 3-state; inverting

74HC/HCT563

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT							
D _n	0.35							
LE	0.65							
ŌĒ	1.25							

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
SYMBOL			74HCT								
		+25			-40 to +85		-40 to +125		UNIT	V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(-,	
t _{PHL} / t _{PLH}	propagation delay D_n to \overline{Q}_n		18	30		38		45	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay LE to \overline{Q}_n		19	35		44		53	ns	4.5	Fig.7
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} to \overline{Q}_n		20	35		44		53	ns	4.5	Fig.8
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} to \overline{Q}_n		22	35		44		53	ns	4.5	Fig.8
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6
t _W	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig.7
t _{su}	set-up time D _n to LE	10	3		13		15		ns	4.5	Fig.9
t _h	hold time D _n to LE	5	-1		5		5		ns	4.5	Fig.9

Octal D-type transparent latch; 3-state; inverting

74HC/HCT563

AC WAVEFORMS

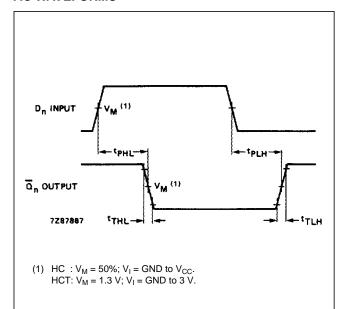
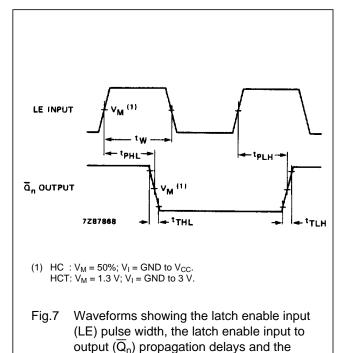
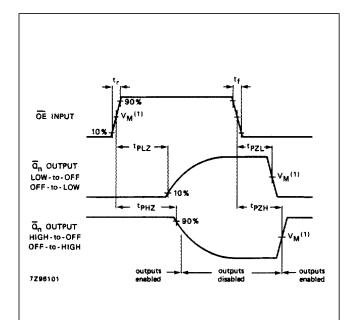


Fig.6 Waveforms showing the data input (D_n) to output (\overline{Q}_n) propagation delays and the output transition times.

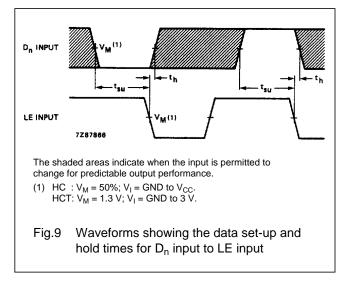


output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the 3-state enable and disable times.



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".